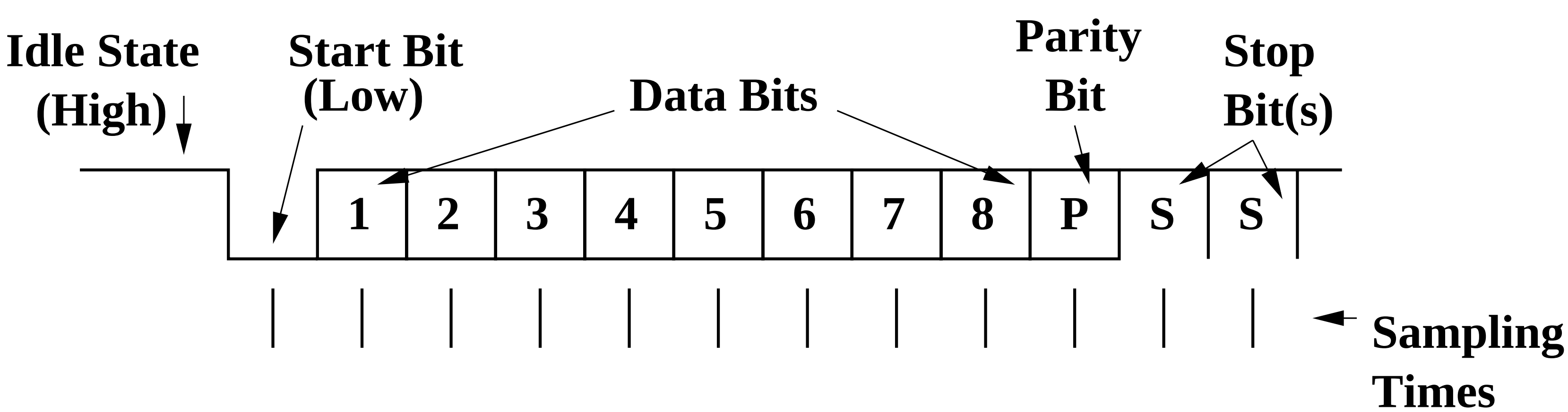
Data Transmission and Video

Data Transmission

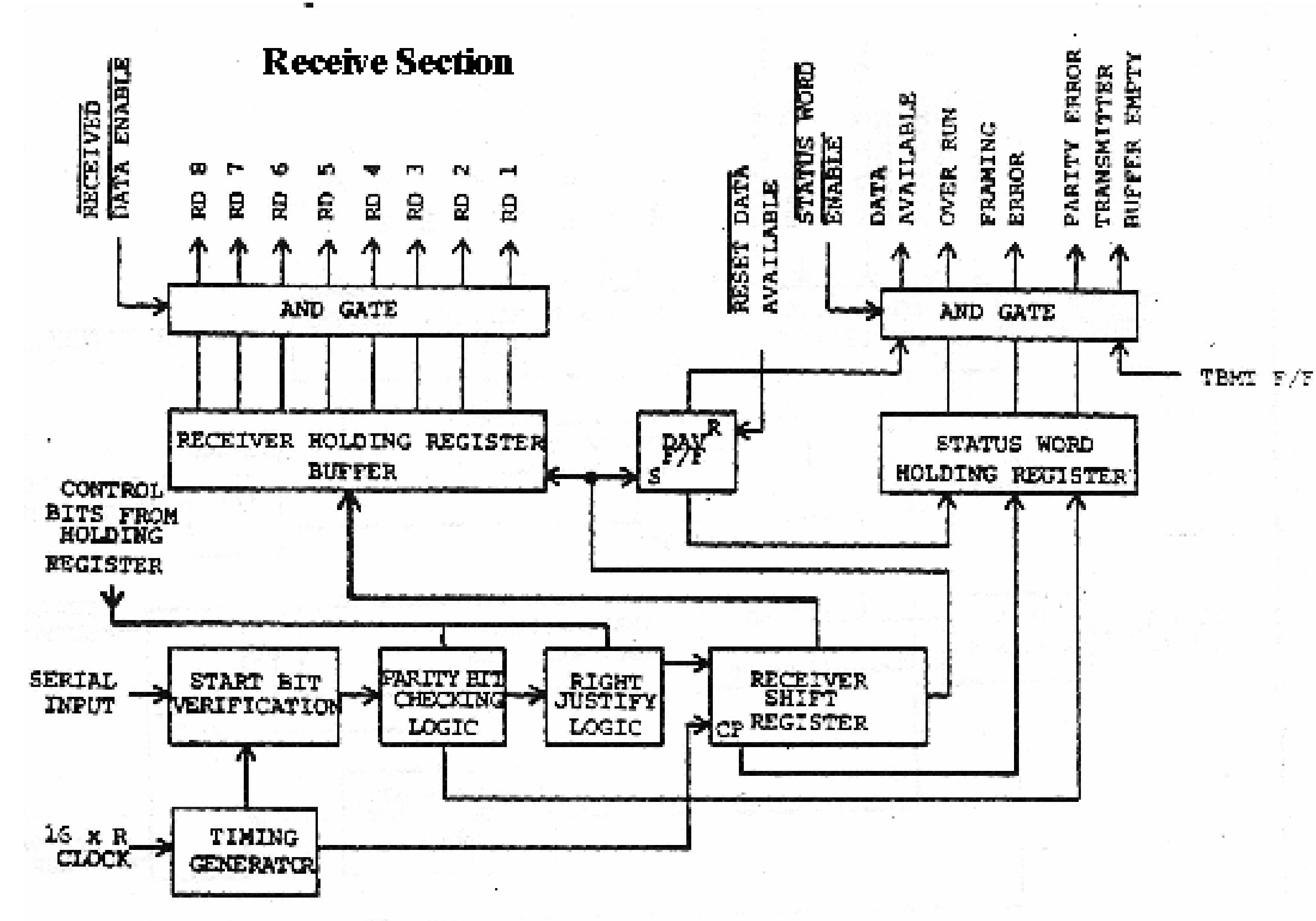
- There are two basic methods.
  - Recover a clock from a serial transmission.
    - This requires a phase lock loop.
    - Examples:
      - network data
      - disk
      - tape
      - GPS
      - Digital TV
    - We will not do this in 6.111.
      - FPGAs are hardwired to use a single clock.
  - Synchronize incoming data to a local clock.
    - Serial data transmission
      - Uses only two wires (or radio and earth ground).
      - Slow – at most one bit per clock period
    - Parallel data transmission
      - Uses at least one wire per bit.
      - Fast – a word (n bits) at a time
      - Need to agree on control signals to know when data is stable

Serial Data Transmission

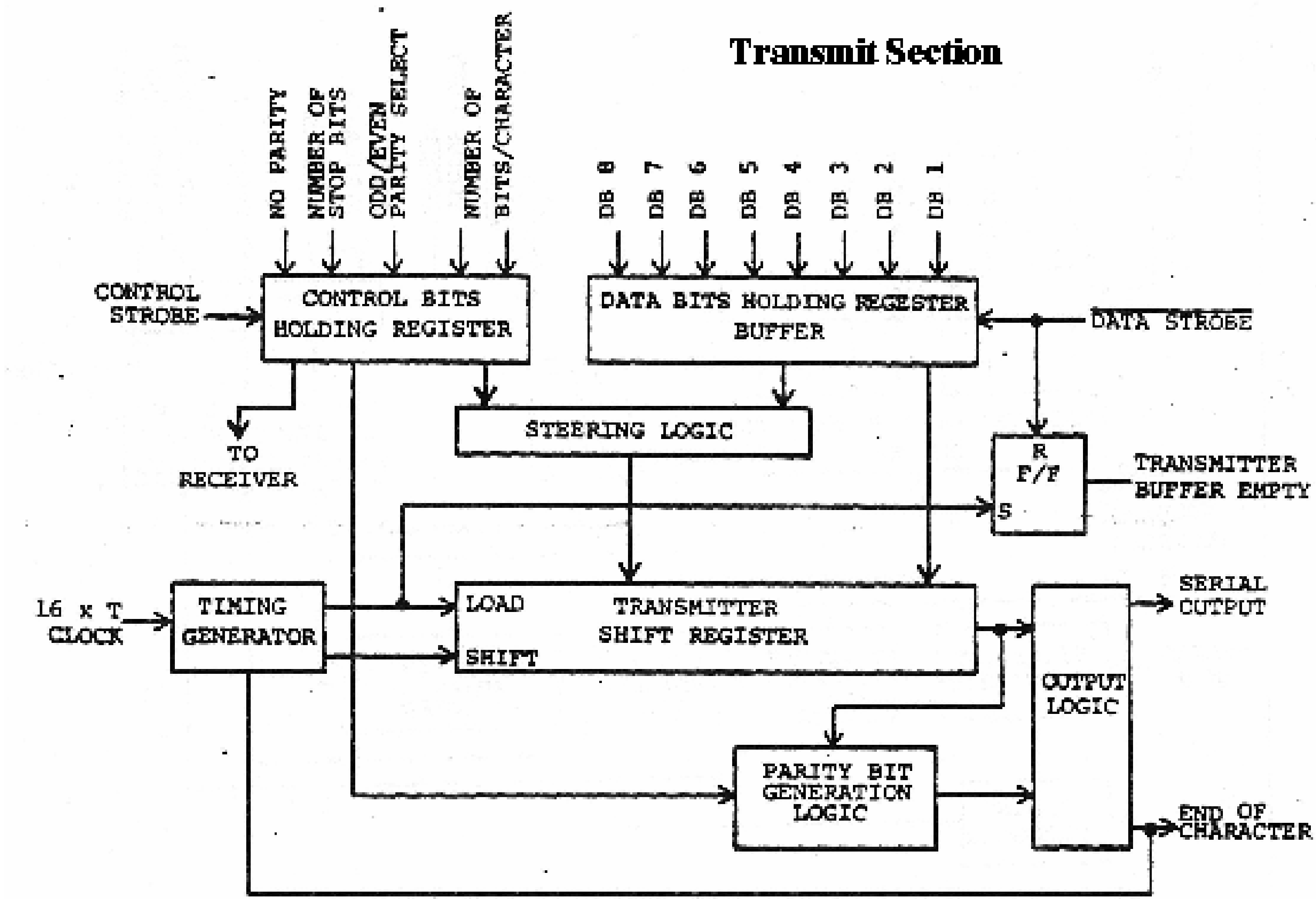
- **RS – 232 is a serial interface standard.**
  - **RS – 232 levels are between**
    - **- 3v and – 15 v for a logic 1**
    - **+ 3v and + 15 v for a logic 0**
- **The TTL signal below has an "idle" state of a logic 1.**
  - **MAXIM 233 has two RS – 232 to TTL and two TTL to RS – 232 level converters.**



AY-3-1015D Receive Section



AY-3-1015D Transmit Section

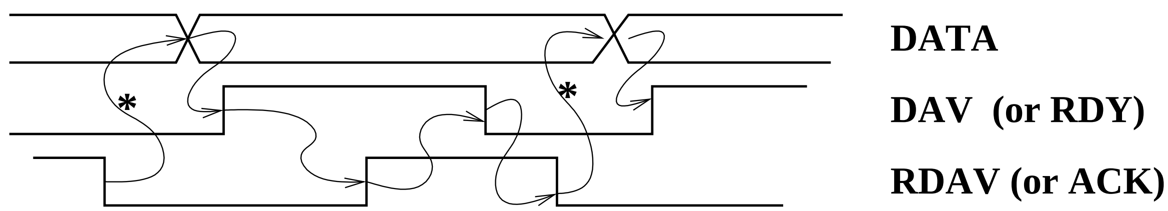


Do Not Use the AY-3-1015D

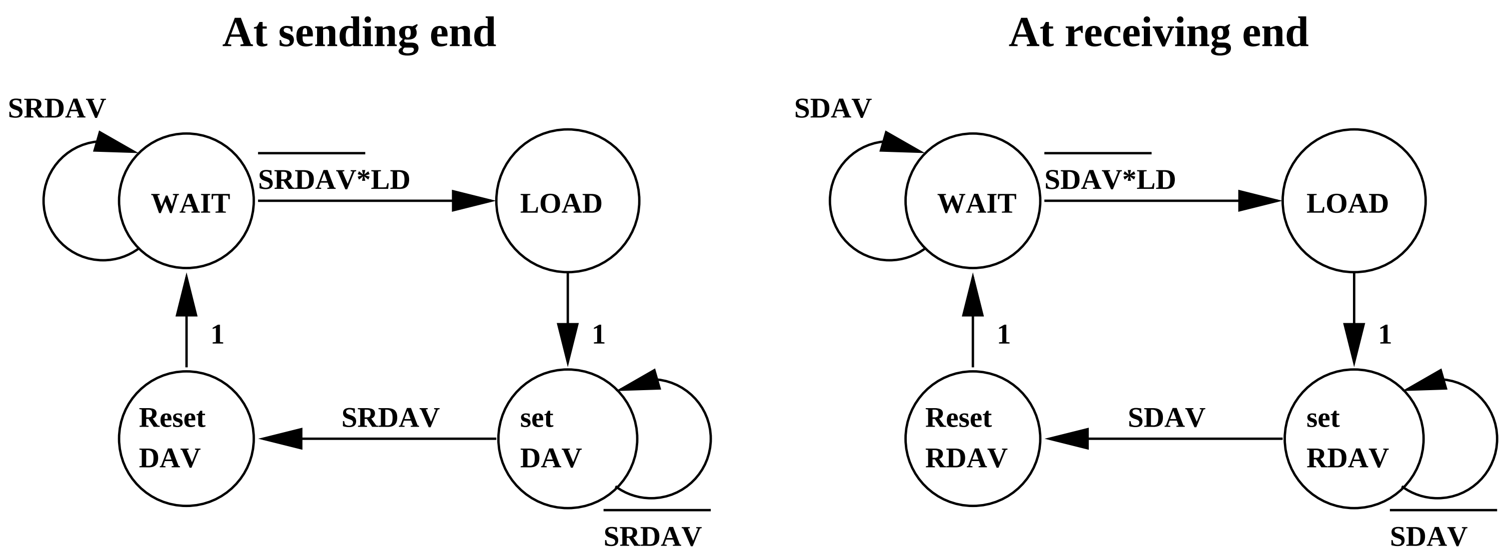
- Well, use it as a guide to coding your desired function in VHDL.
- Transmitter
  - You likely do not need the Control Bits Holding Register.
    - Do you want odd or even or no parity?
    - What about stop bits?
  - Do you need to double buffer the input data?
  - What will you use for a timing generator?
- Receiver
  - Do you have to synchronize the received data?
  - What error outputs do you need?
  - Do you need to verify the start bit?
  - When do you start shifting the data?
  - Do you need to double buffer the received data?

Parallel Transmission

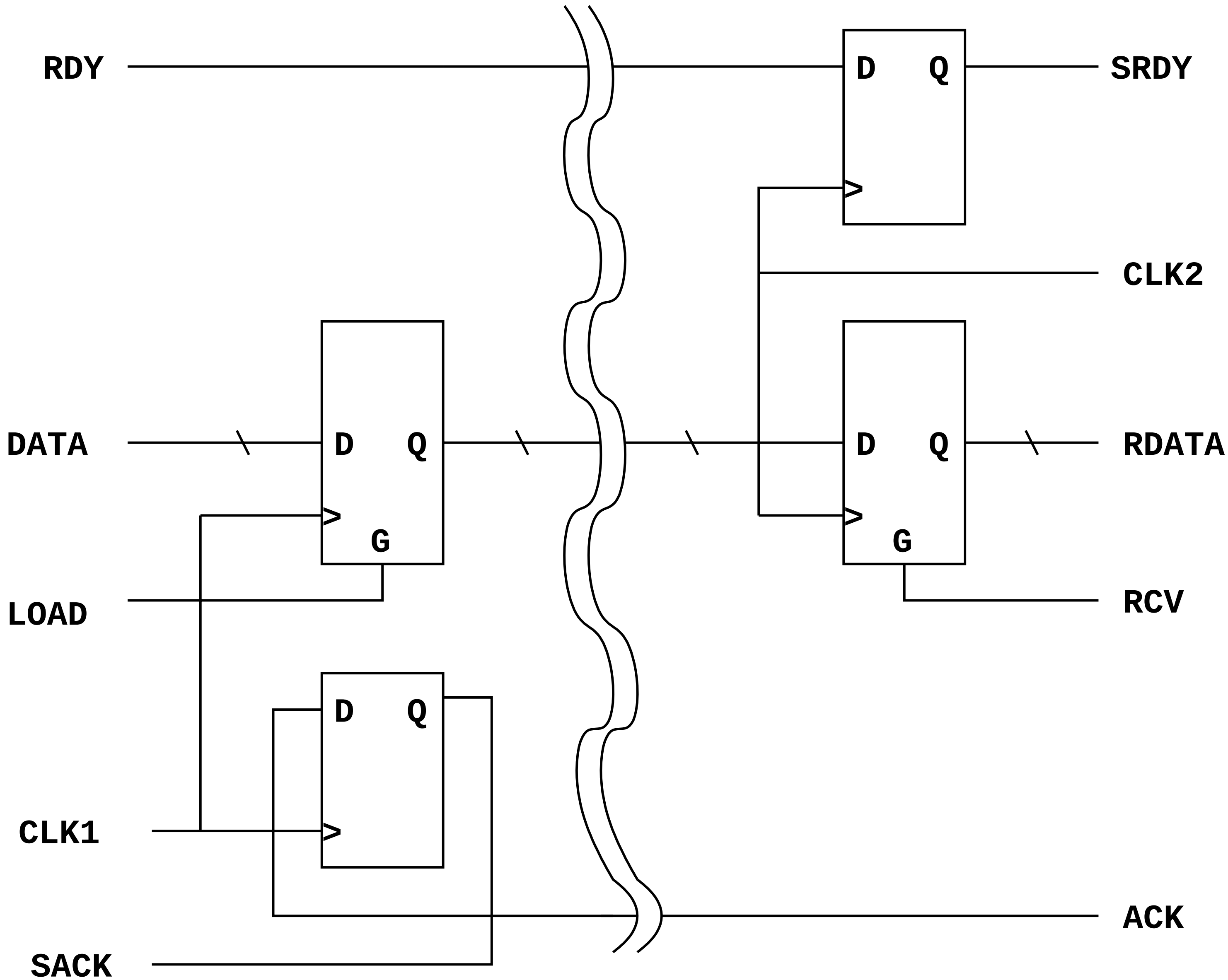
- **Full Handshake – RDY and ACK return to zero.**
  - Assumes data source and destination have unrelated clocks.
  - E.g., the two locations are on separate kits.
  - Why not send clock from one kit to another?



*** and we want to send more data, i.e., LD is true.**

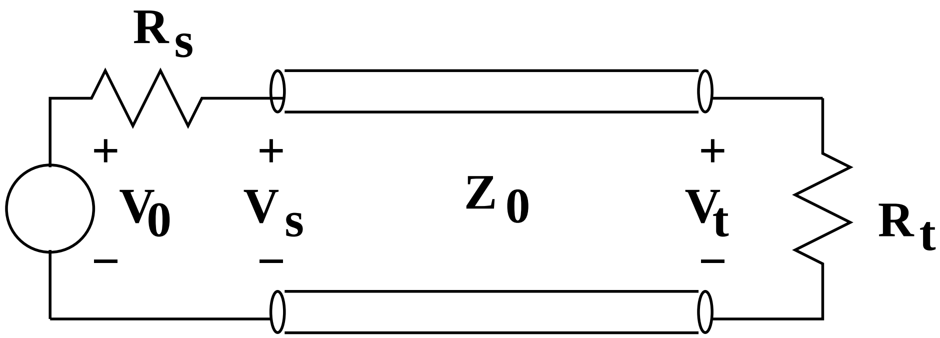


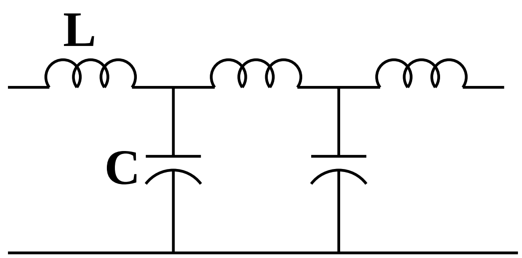
Parallel Interface



Transmission Lines

- Signals travel on wires.
  - Attenuation – losses due to resistance of wires
  - Reflections – affected by terminations





Transmission line has characteristic parameters:

L: Inductance per unit length
C: Capacitance per unit length

$$Z_0 = \sqrt{\frac{L}{C}}$$

Z_0 : Characteristic Impedance

U_0 : Phase Velocity

$$U_0 = \sqrt{\frac{1}{L\,C}}$$

Signal Propagation

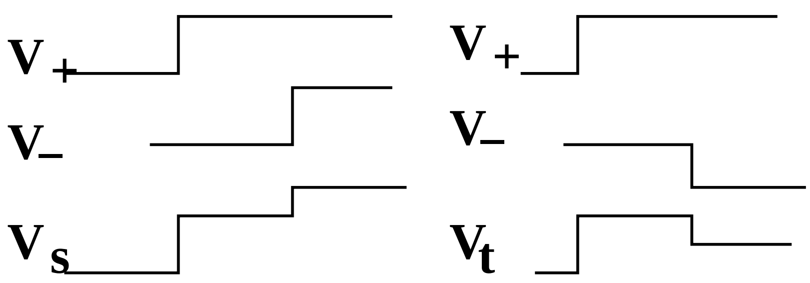
- **Pulses travel along the line.**
  - **Ratio of voltage to current is the “characteristic impedance”.**
  - **Sign of that ratio is the direction of propagation.**
  - **Pulses propagate at a velocity < c (speed of light).**

$$V_+ = Z_0 \, I_+ \qquad\qquad V_- = -Z_0 \, I_-$$

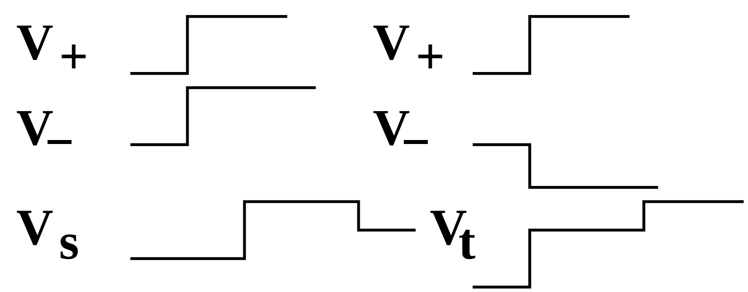
Reflections

- Pulses are absorbed if the receiving end is matched to the characteristic impedance.
  - If the receiving end is not matched then a pulse “reflects”.
  - The sign of the reflection depends on the impedance value relative to the characteristic impedance.

Reflections: $R_t > Z_0$

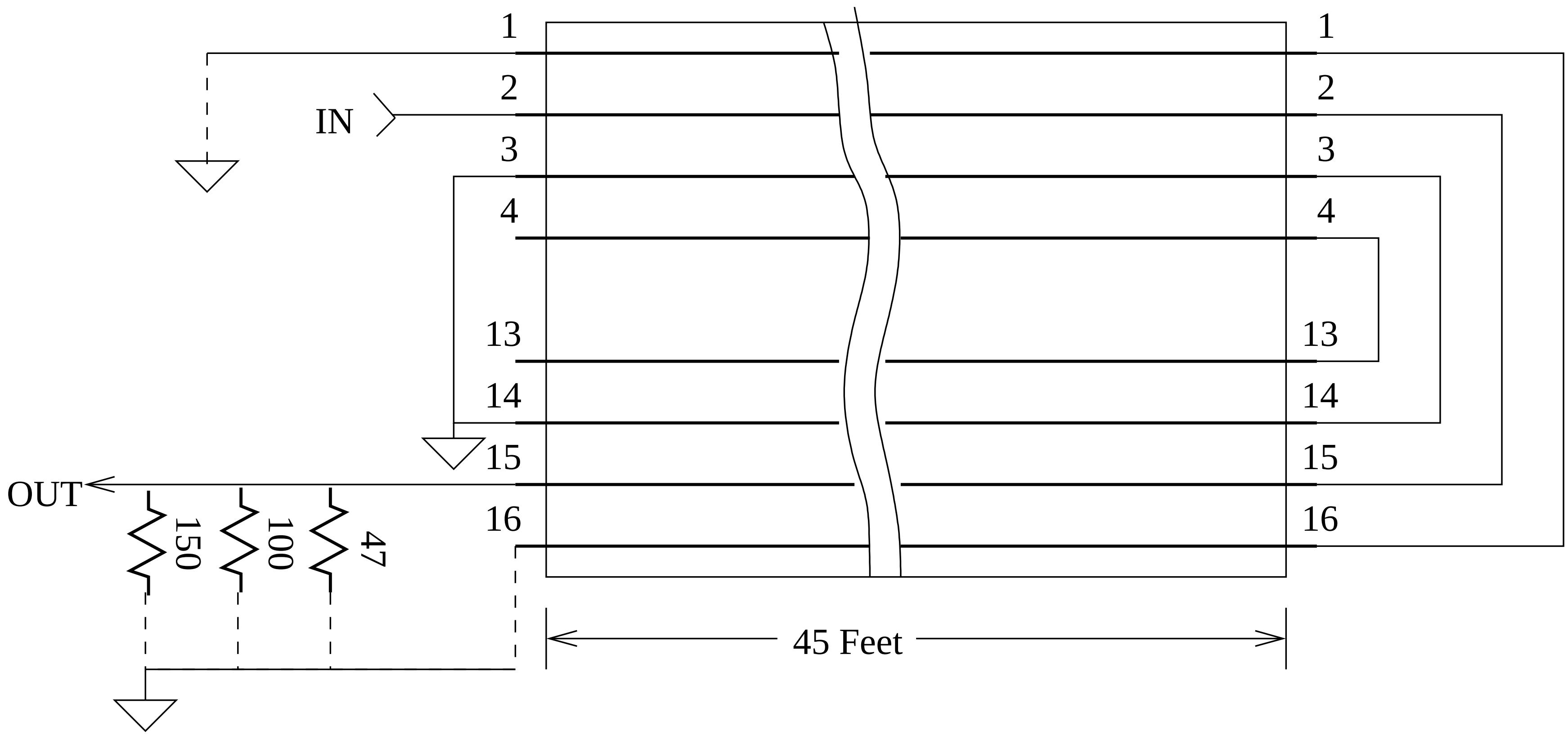


Reflections: $R_t < Z_0$



Characteristic Impedance Demo

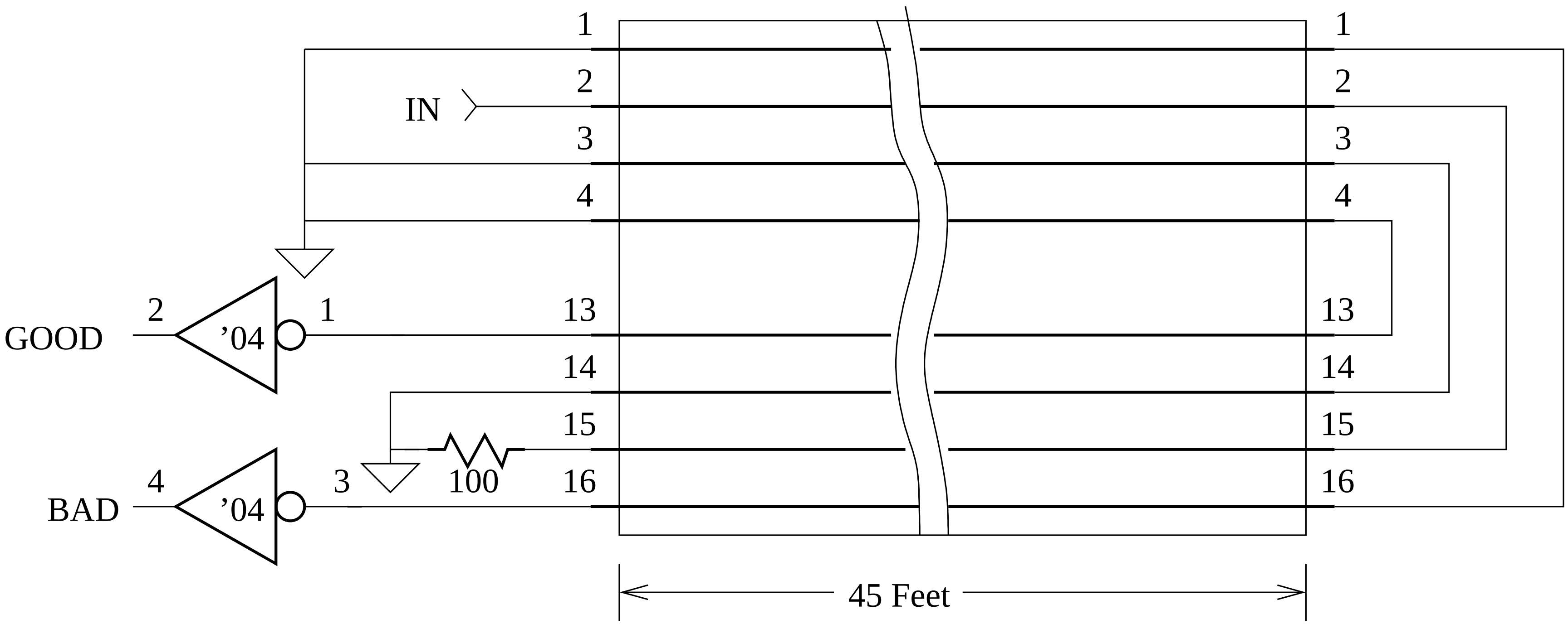
- **Reflections depend on the terminating impedance.**
  - **They can be minimized by terminating correctly, i.e., with the characteristic impedance?**
  - **Why can't they be eliminated?**



Moral: Terminate Wires in Characteristic Impedance

Crosstalk Demo

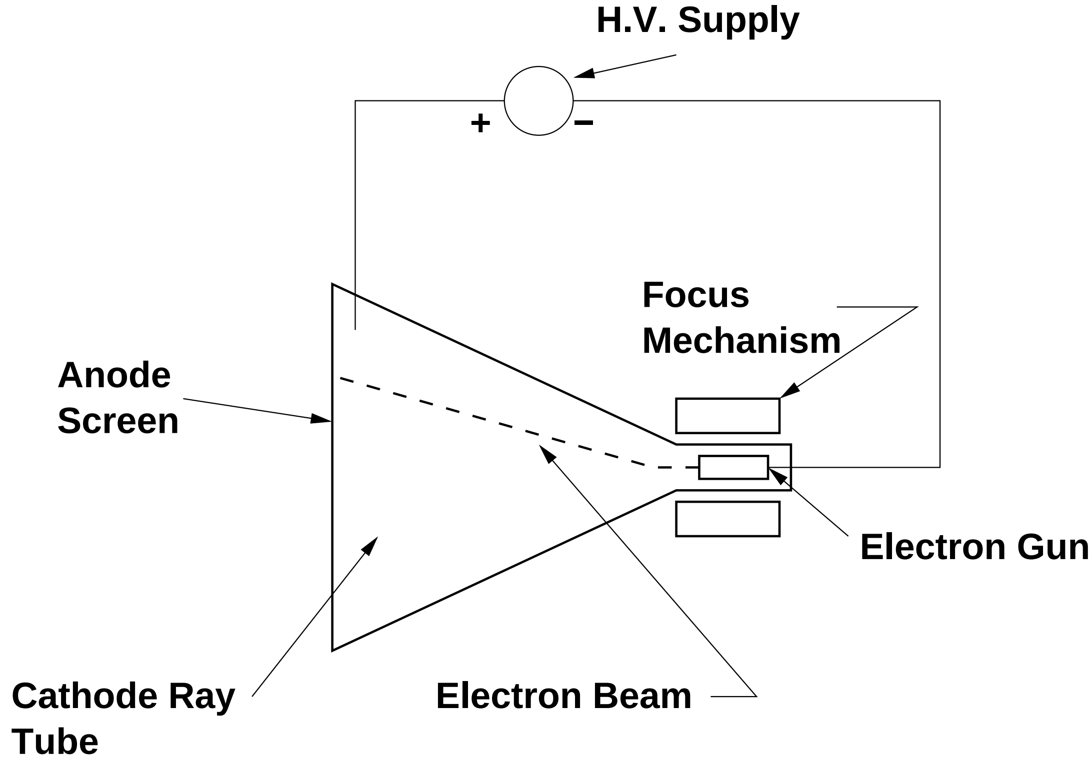
- Flat ribbon cable – similar to kit interconnect cables
  - The wires are situated right next to each other.
  - They have capacitive and inductive coupling.
- Crosstalk is minimized by alternating signals and grounds.
  - Ground – Signal – Ground – Signal ……



Moral: Alternate Ground and Signal Wires in Cables

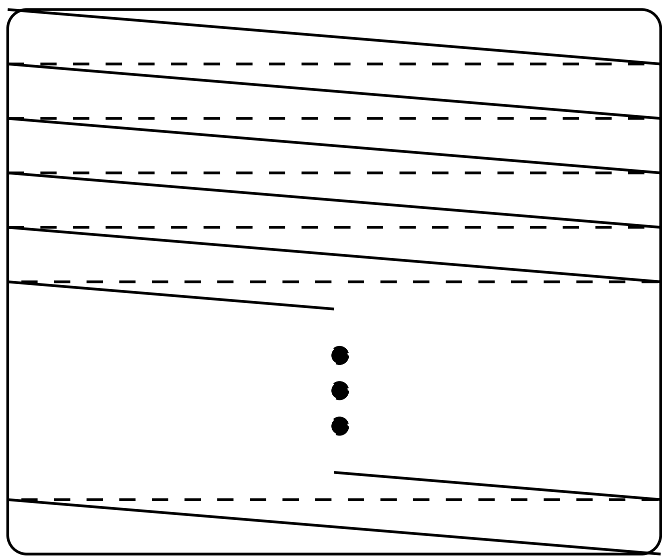
Video Displays

- Video displays are implemented by mirrors, LCDs, and CRTs.
- In a CRT (the displays in our laboratory)
  electron beams are focused on a small spot on the screen.
  The energy delivered to a phosphor causes a dot (pixel) to glow.
  - The beam can be moved rapidly in two dimensions.
  - The beam current determines the brightness of the spot.



Raster Scan

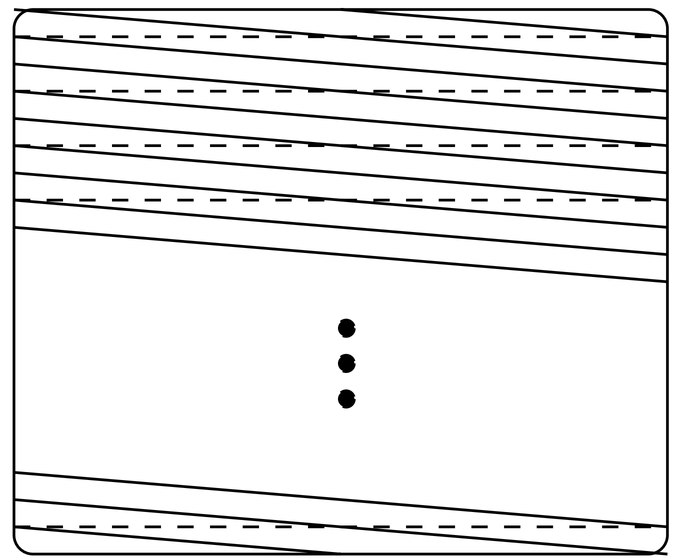
- **Television and most computer displays use raster scan.**



Non−Interlaced: Frame rate may be 60, 72, etc. frames/sec.

———— Scan line

- - - - - - Retrace line

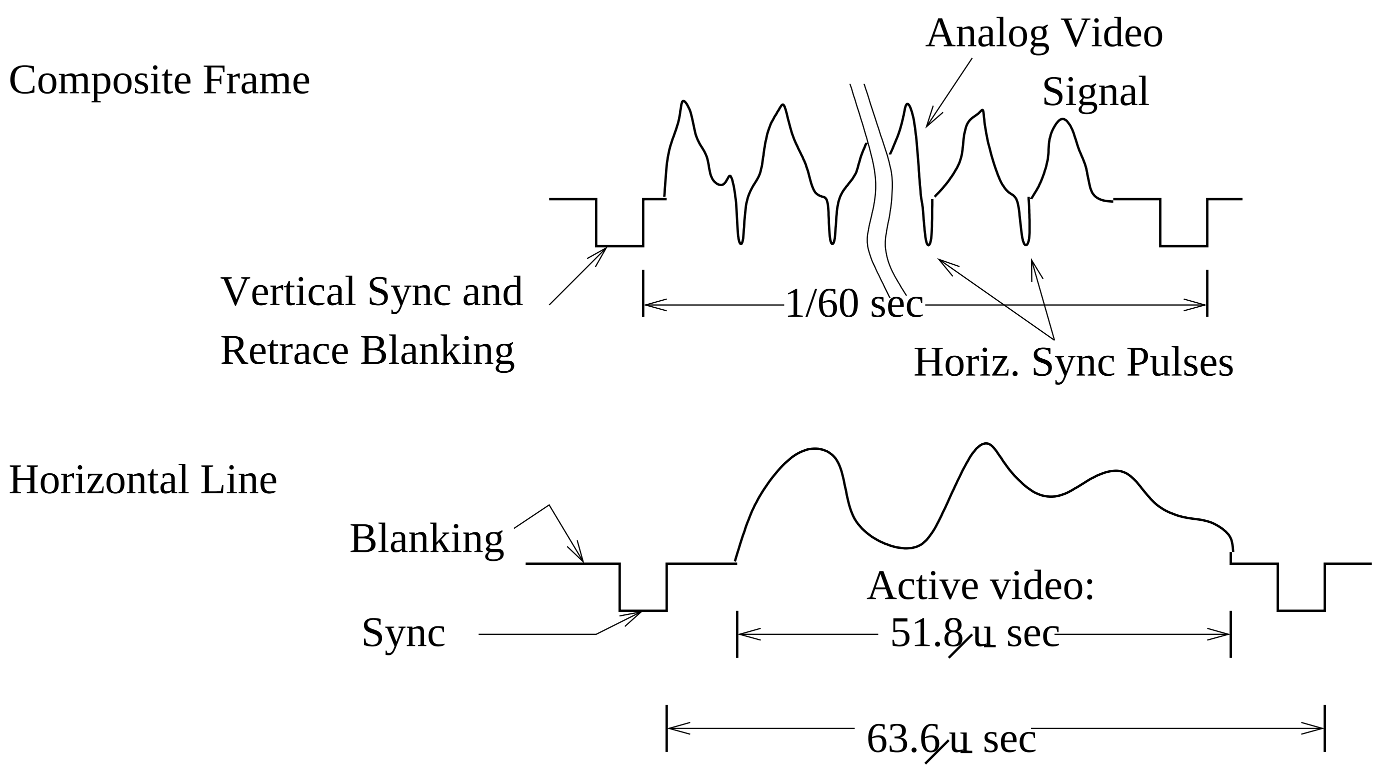


Interlaced: Frames alternate. This is like television: 60 half frames/sec.

Electron beam "scans" tube. Beam location is shown here. Beam current determines brightness of display.

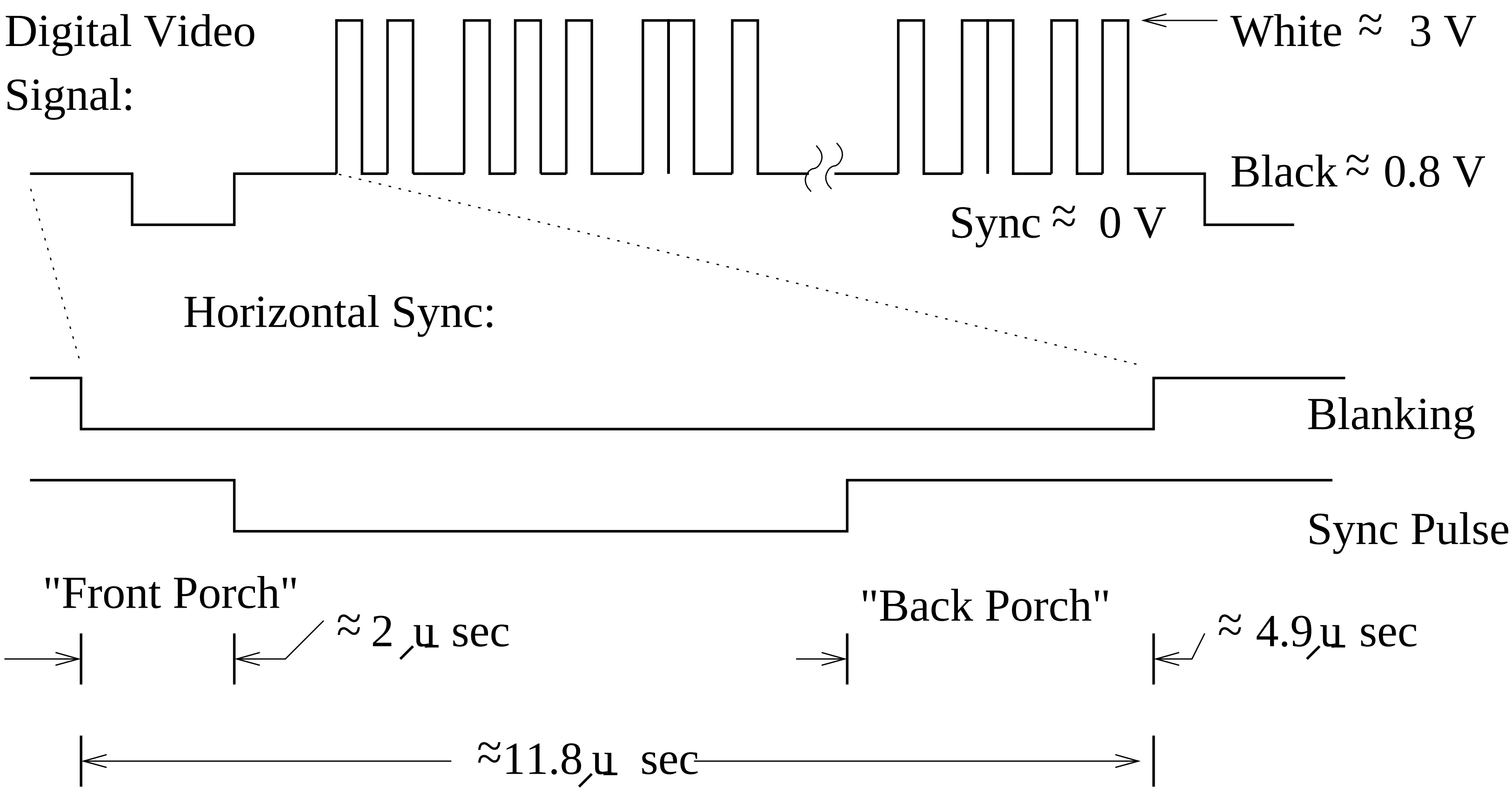
Composite Frames

- **The 'frame' is a single picture (snapshot).**
  - **It is made up of many lines.**
  - **Each frame has a synchronizing pulse (vertical sync).**
  - **Each line has a synchronizing pulse (horizontal sync).**
  - **Brightness is represented by a positive voltage.**
  - **Horizontal and Vertical intervals both have blanking so that retraces are not seen (invisible).**



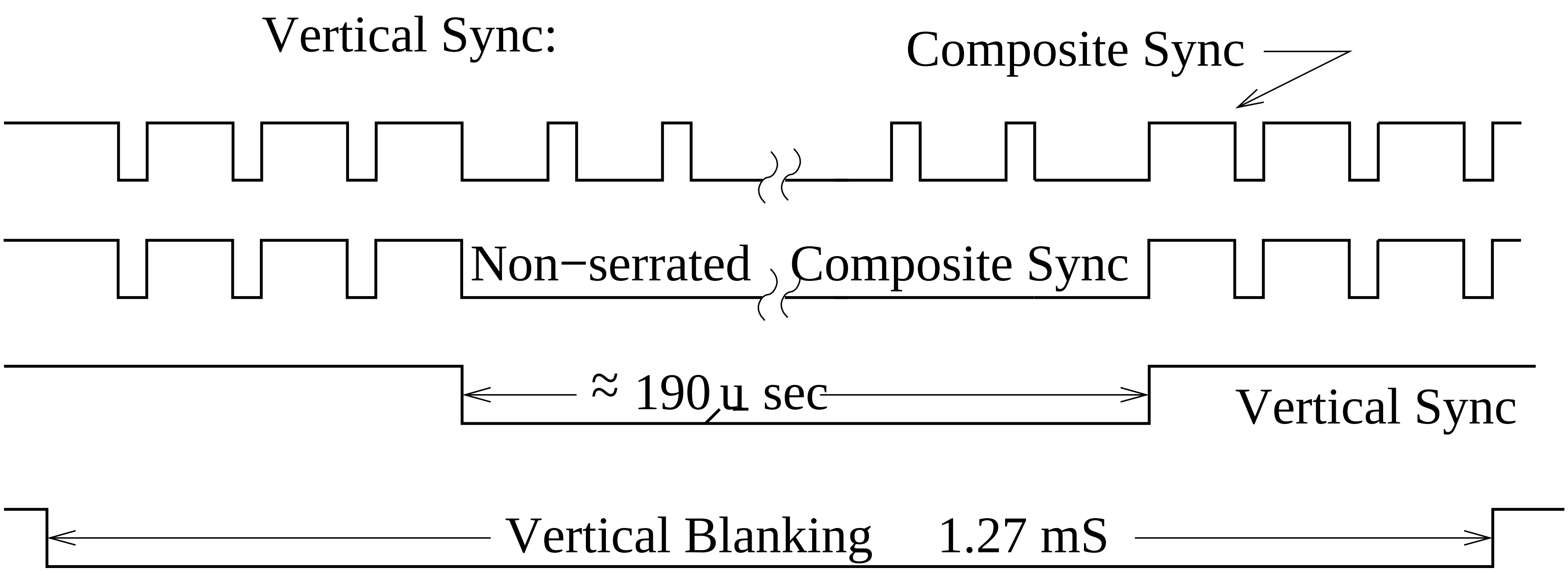
Synchronization

- **The picture consists of white dots on a black screen.**
  - **White is the highest voltage.**
  - **Black is a low voltage.**
  - **Sync is below the black voltage.**
- **Sync pulses are surrounded by the blanking interval so one does not see the retrace.**



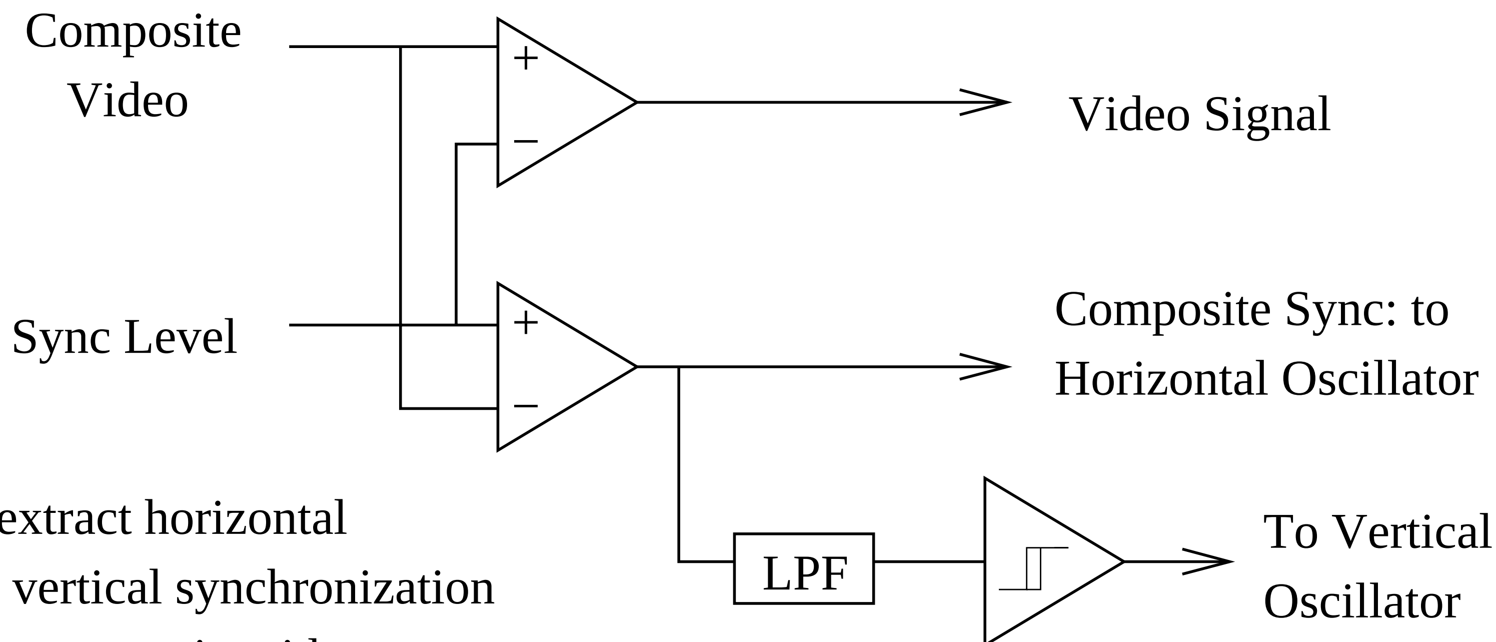
Composite Synchronization

- Horizontal sync coordinates lines.
- Vertical sync coordinates frames.
- They are similar except for the time scales and they are superimposed on each other. The numbers are for TV like displays.
  - What purpose is there for serrated sync?



(Conceptual) Recovery of Signals

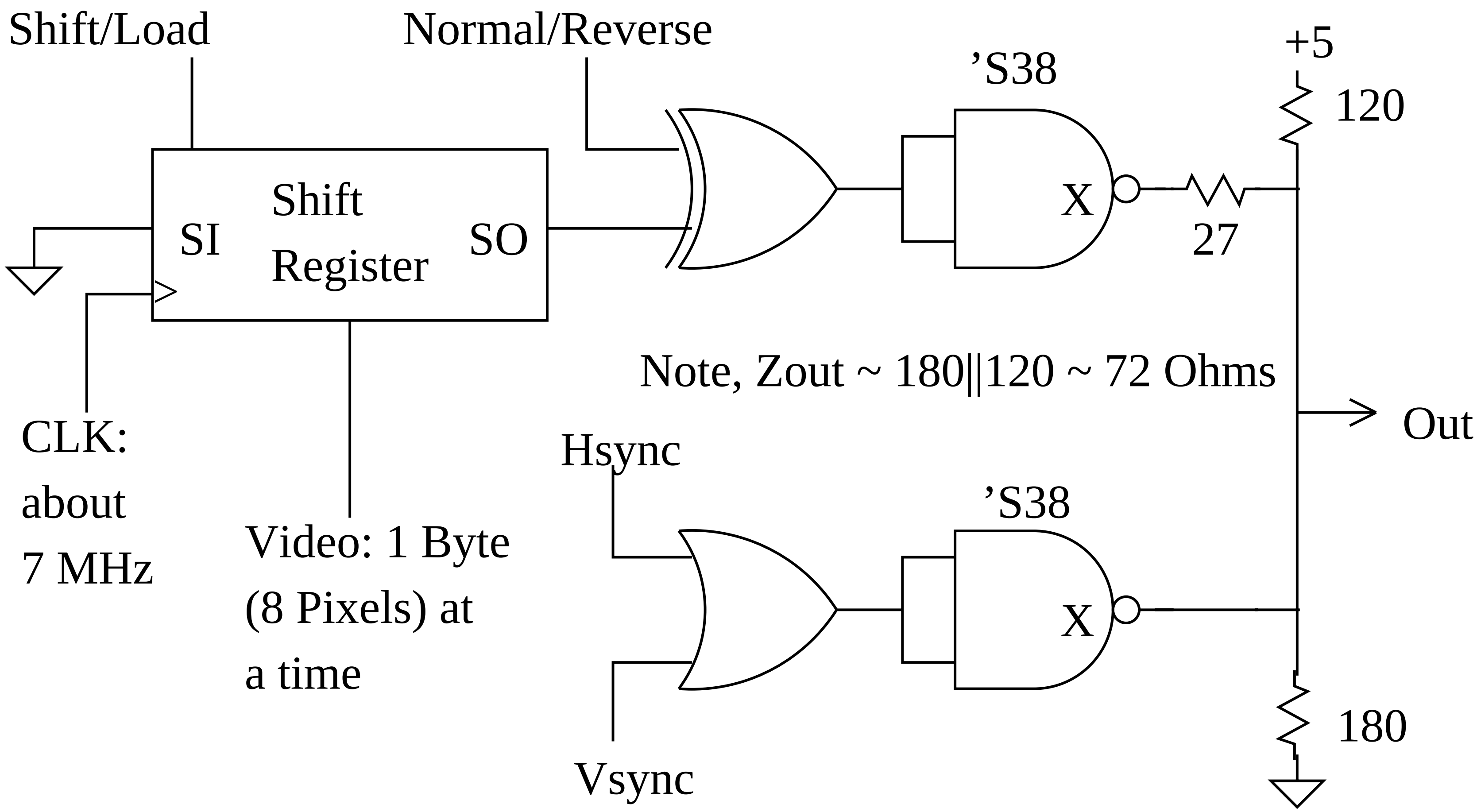
- **Composite video has picture data and both syncs.**
  - **Picture data (video) is above the sync level.**
  - **Simple comparators extract video and composite sync.**
- **Composite sync is fed directly to the horizontal oscillator.**
- **A low-pass filter is used to separate the vertical sync.**
  - **The edges of the low-passed vertical sync are squared up by a Schmidt trigger.**



To extract horizontal and vertical synchronization from composite video

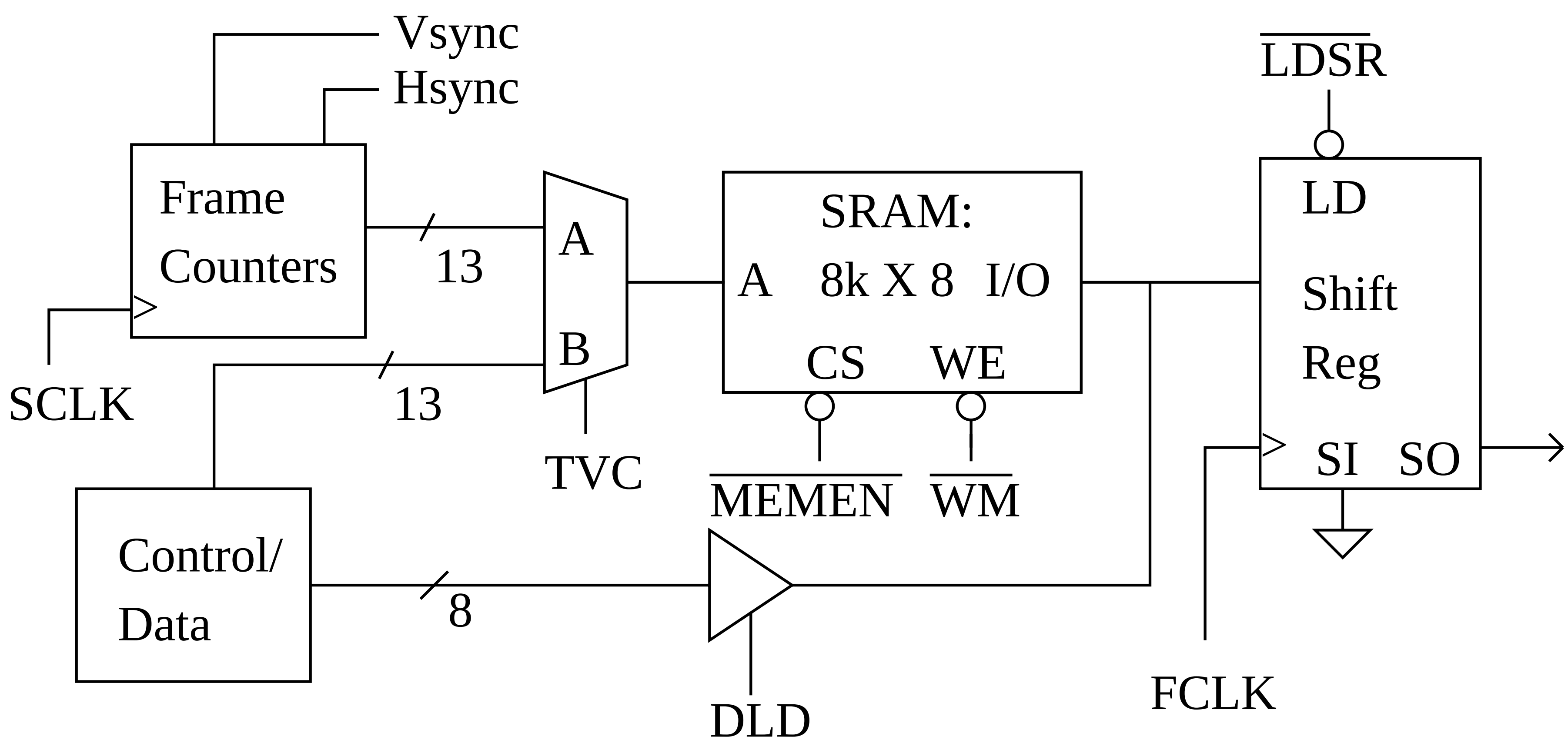
Generation of Signals

- Assume one bit per pixel and provide for reverse video.
- This is a simple 'D/A' to generate monochrome signals.
  - The 'S38 is an open collector part so the voltages are determined by the resistor network. The output resistance is ~ 75 ohms.



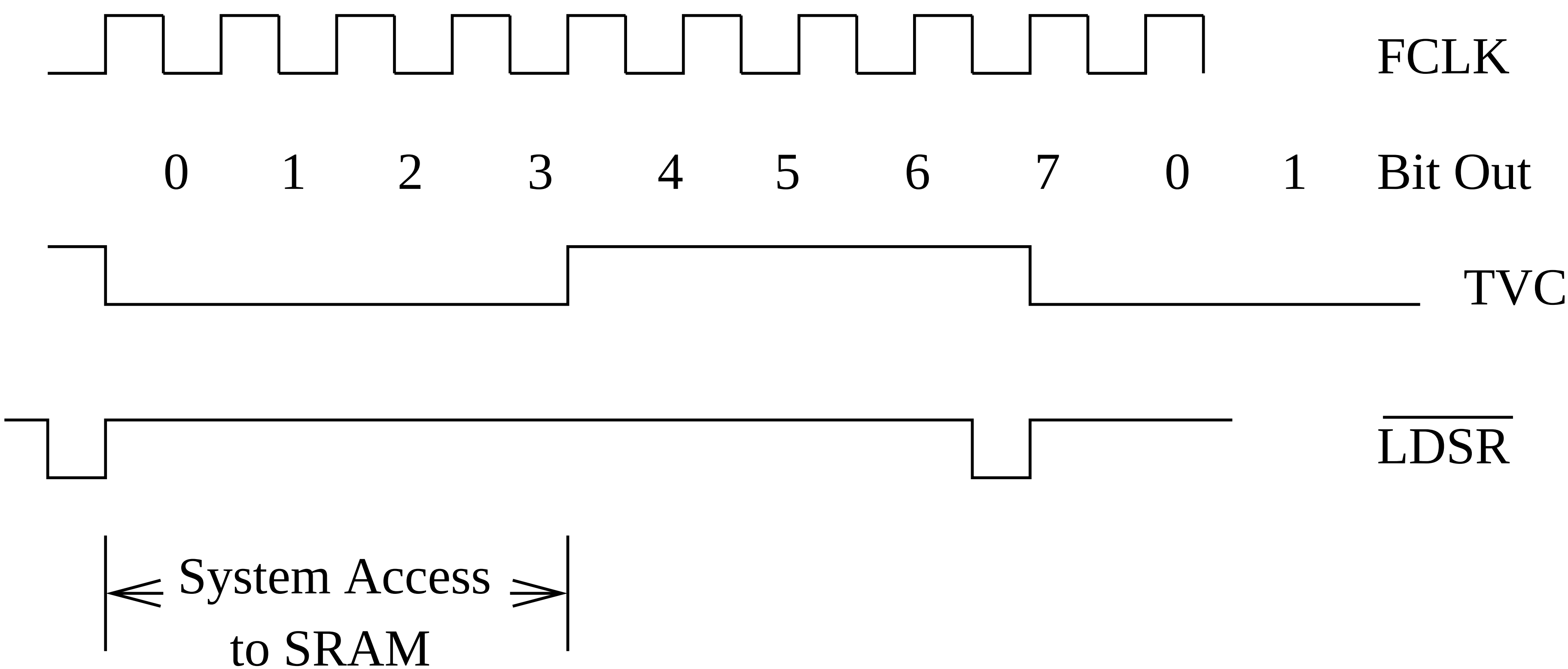
Control

- Here is one possible display format.
  - 256 pixels X 192 rows
  - 7.16 MHz clock => 140 nanoseconds per pixel
  - Display time for the active line is 35.8 microseconds.
  - 256 X 192 = 49,152 = 48K pixels = 6 K bytes



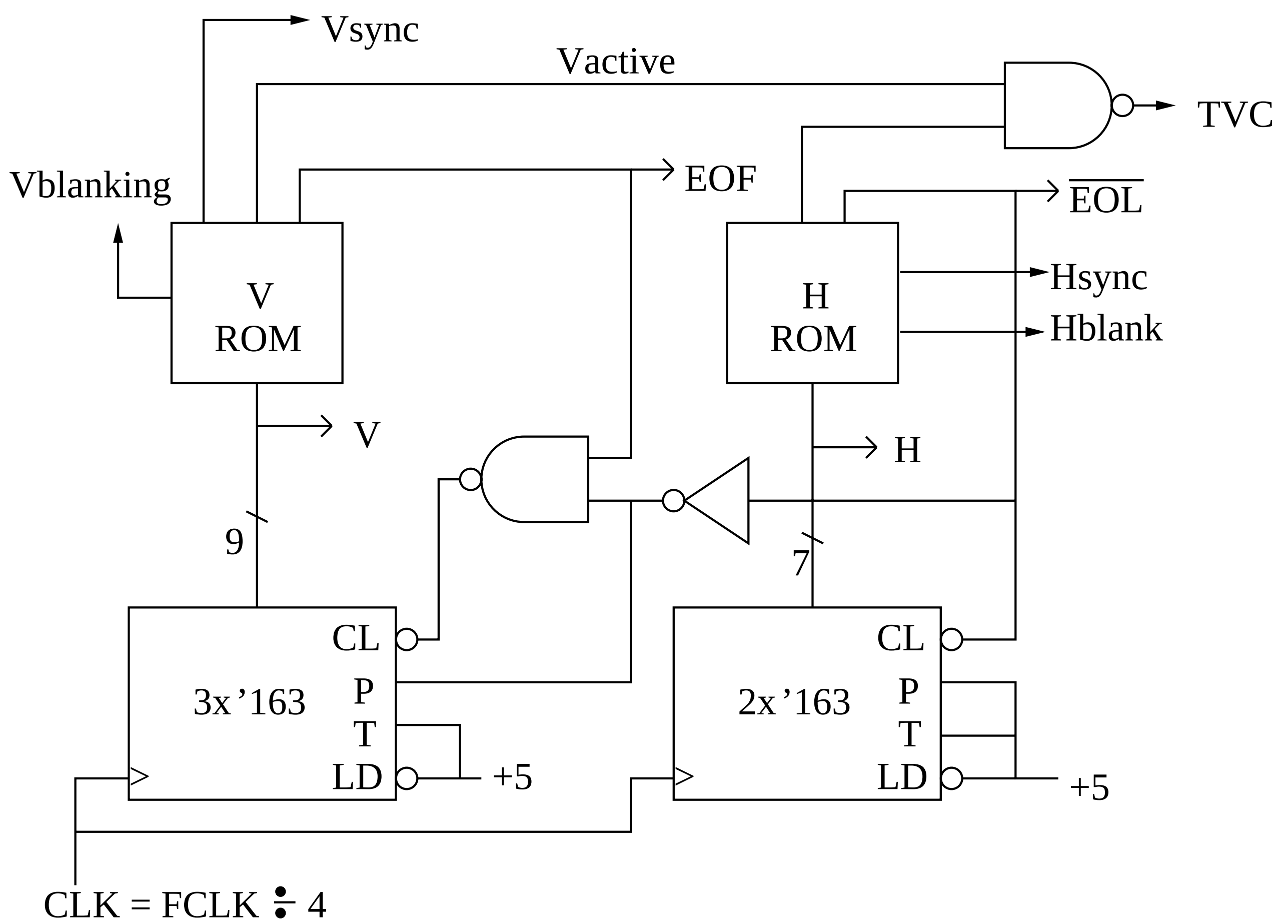
Timing of Control Signals

- **Data is loaded into a shift register and shifted out to generate the video signal.**
  - **FCLK is at the pixel rate.**
  - **TVC divides access to the SRAM giving half the time to get data to load into the shift register .**



Generation of Control Signals

- **Here is one way to generate control signals**
  - **by storing information in ROMs to generate sync signals, TVC, and /EOL.**
  - **Note that EOL cause a line count and /EOL clears the dot counter.**
  - **And that (EOF AND EOL) causes a clear of the line counter.**



ROM Contents for Control

- **Vertical Rom**

Number of words	Addresses	Contents
192	0 – 191	Vactive
26	192 – 217	Vblanking
6	218 – 223	Vsync
37	224 – 260	Vblanking
1	261	EOF

- **Horizontal ROM**

Number of words	Addresses	Contents
32	0- 31	Hactive
9	32- 40	Hblanking
7	41- 47	Hsync
8	48- 55	Hblanking
1	56	EOL

- **Whoops! Make sure the EOL bit is negative true.**

