



L4: Construction and Analysis of Sequential Building Blocks



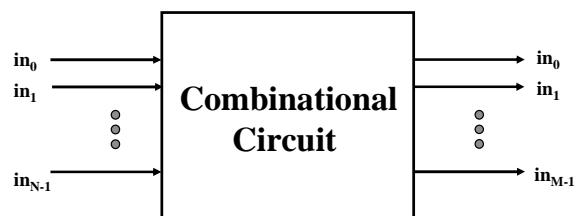
Some (most) lecture material derived from R. Katz, "*Contemporary Logic Design*", Addison Wesley Publishing Company, Reading, MA, 1993. *Some slides are derived from slides used in past terms of 6.111*

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Combinational Logic Review



No feedback in combinational circuits

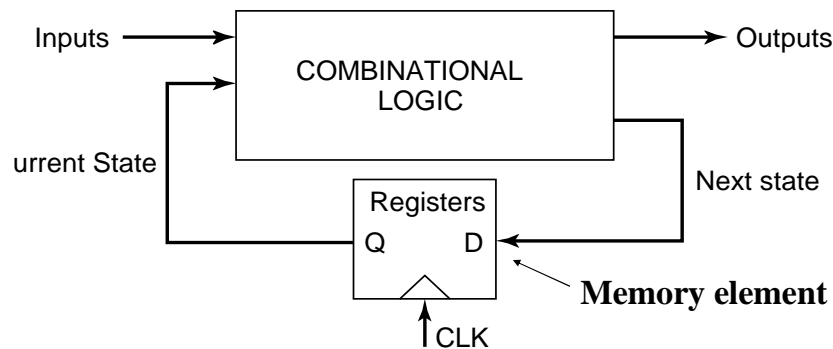
- **Combinational logic circuits are memoryless.**
- **There is no feedback from inputs and outputs.**
- **The output assumes the function implemented by the logic network, assuming that the switching transients have settled.**

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A Sequential System



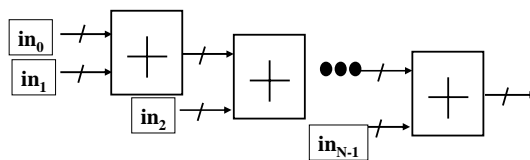
- Sequential circuits have memory (i.e., remember the past).
- The current state is “held” in memory and the next state is computed based on the current state and the current inputs.
- In a synchronous system, the clock signal orchestrates the sequence of events.



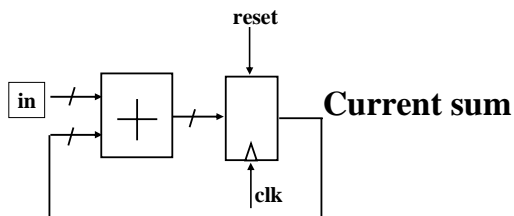
A Simple Example



Adding N inputs (N-1 Adders)

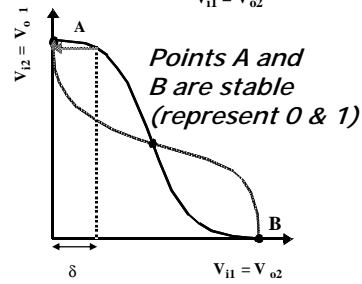
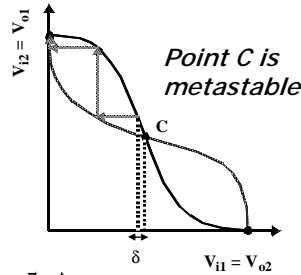
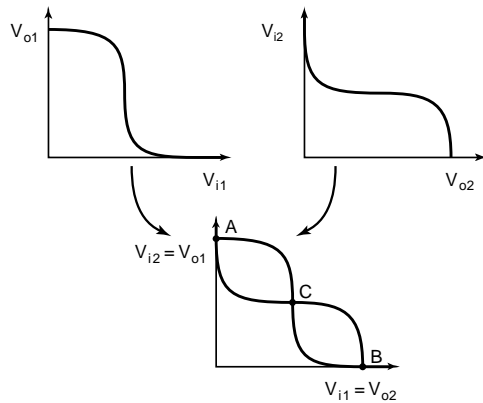
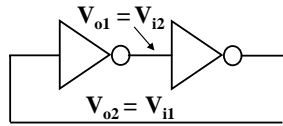


Using a sequential (serial) approach

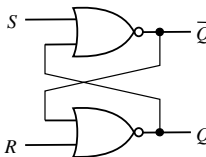
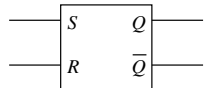




Implementing State: Bi-stability

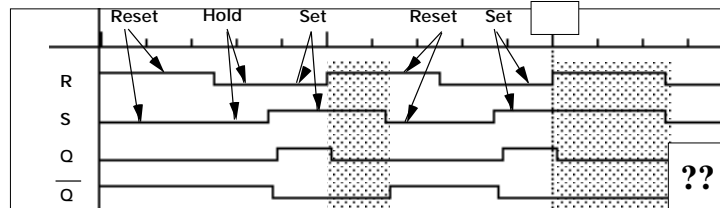
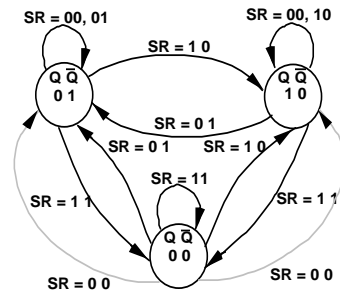


NOR-based Set-Reset (SR) Flip-Flop



S	R	Q	\bar{Q}
0	0	Q	\bar{Q}
1	0	1	0
0	1	0	1
1	1	0	0

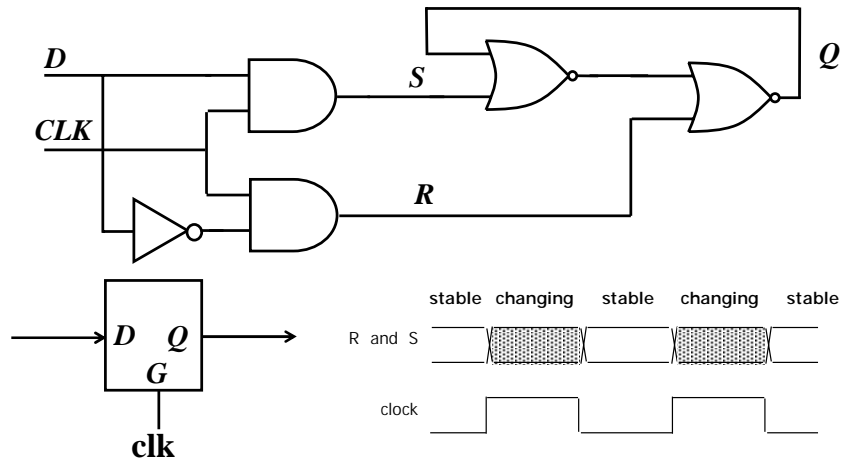
Forbidden State



- Flip-flop refers to a bi-stable element (edge-triggered registers are also called flip-flops). This circuit is not clocked and outputs change “asynchronously” with the inputs.



Making a Clocked Memory Element: Positive D-Latch



- A Positive D-Latch: passes input D to Q when clk is high and holds state when clock is low (i.e., ignores input D).
- A Latch is level-sensitive: invert clock for a negative latch.

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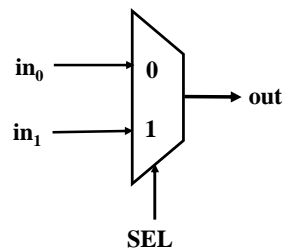
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Multiplexor Based Positive & Negative Latch

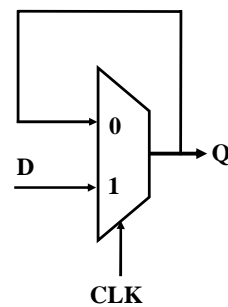


2:1 multiplexor

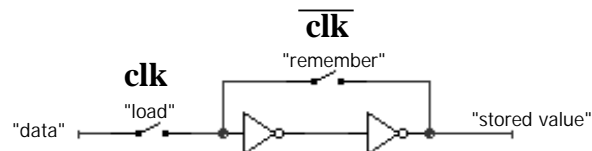
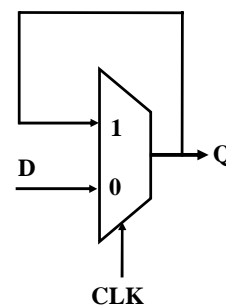


$$\text{Out} = \text{sel} * in_1 + \overline{\text{sel}} * in_0$$

Positive Latch



Negative Latch

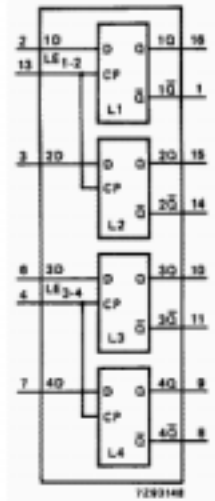


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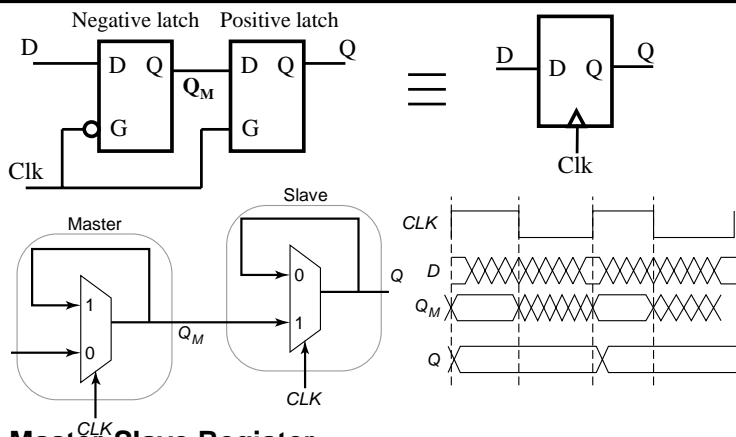
74HC75 (Positive Latch)



OPERATING MODES	INPUTS		OUTPUTS	
	LE_{n-1}	nD	nQ	$n\bar{Q}$
data enabled	H	L	L	H
	H	H	H	L
data latched	L	X	q	\bar{q}



Building an Edge-Triggered Register



■ Master-Slave Register

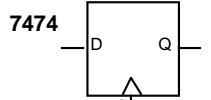
- Use negative clock phase to latch inputs into first latch.
- Use positive clock phase to change outputs with second latch.

■ View pair as one basic unit.

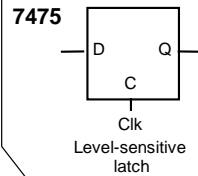
- master-slave flip-flop twice as much logic



Latches vs. Edge-Triggered Register



7474
Positive edge-triggered register

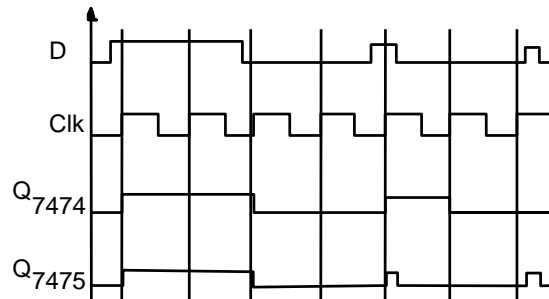


7475
Level-sensitive latch
Bubble here for negative edge-triggered register

Edge-triggered devices sample inputs on the event edge.

Transparent latches sample inputs as long as the clock is asserted.

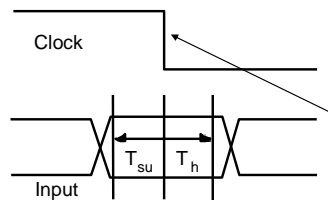
Timing Diagram:



Behavior the same unless input changes while the clock is high



Important Timing Parameters



Clock:

Periodic event, causes state of memory element to change

Memory element can be updated on the rising edge, falling edge, high level, low level.

Setup Time (T_{su})

Minimum time before the clocking event by which the input must be stable

Hold Time (T_h)

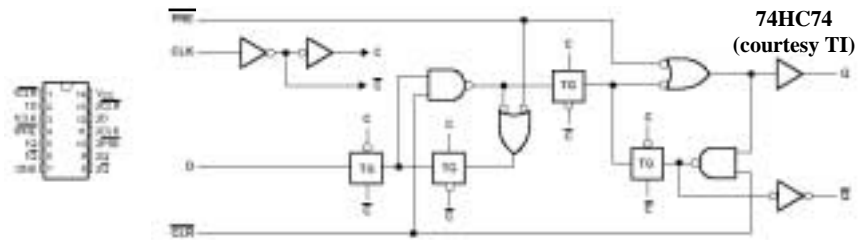
Minimum time after the clocking event during which the input must remain stable

Propagation Delay (T_{cq} for an edge-triggered register and T_{dq} for a latch)

Delay overhead of the memory element

There is a timing "window" around the clocking event during which the input must remain stable and unchanged for the output to be guaranteed.

74HC74 (Positive Edge-Triggered Register)



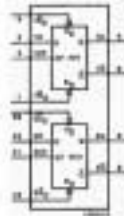
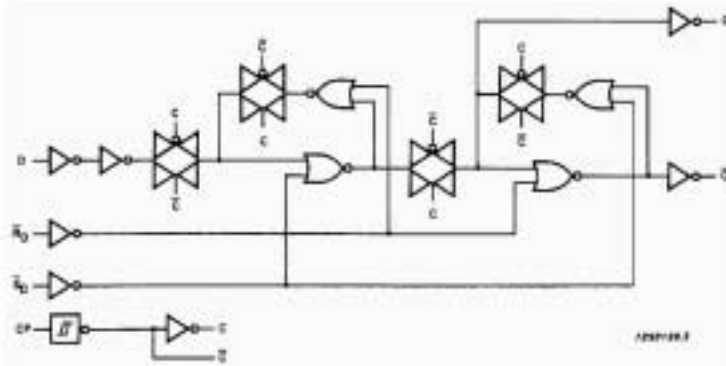
FUNCTION TABLE

INPUTS			OUTPUTS	
PRE	CLR	CLK	Q	Qn
L	H	X	X	L
H	L	X	X	H
L	L	X	X	H [†]
H	H	T	H	L
H	H	T	L	H
H	H	L	X	Q _n

D-FF with preset and clear

	PGC	T ₁ (25°C)		T _{max} (55°C)		UNIT
		MIN	MAX	MIN	MAX	
f _{clk} Clock frequency	2.7	0	0	0	0	MHz
	4.5	0	21	0	25	
	10	0	40	0	25	
t _{pd} Propagation delay	2.7	100	100	100	100	ns
		PRE or CLR to Q		Q to Qn		
	4.5	17	20	21	25	
		CLK high to Q		CLK low to Qn		
	10	15	18	20	22	
		PRE or CLR to Qn		Q to Qn		
t _{su} Setup time before clock	2.7	100	100	100	100	ns
		PRE or CLR to Q		Q to Qn		
	4.5	20	20	20	20	
		PRE or CLR to Qn		Q to Qn		
	10	20	40	20	20	
		PRE or CLR to Q		Q to Qn		
2.7	0	0	0	0	ns	
	PRE or CLR to Q		Q to Qn			
10	0	0	0	0	ns	
	PRE or CLR to Q		Q to Qn			

Philips 74HC74 Implementation

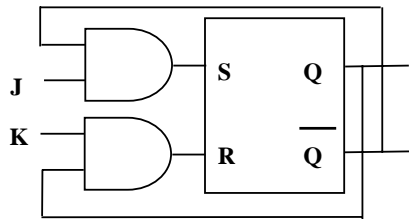


INPUTS			OUTPUTS	
R _n	S	CP	Q	Qn
L	X	X	L	L
L	L	X	L	H

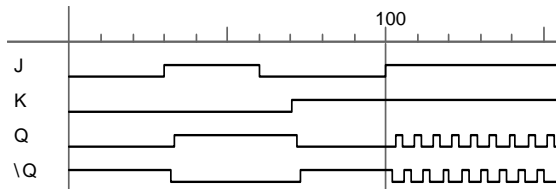
INPUTS			OUTPUTS	
R _n	S	CP	Q _n	Q
H	X	X	H	H
H	H	X	H	L



The JK Flip-Flop



J	K	Q+	\overline{Q} +
0	0	Q	\overline{Q}
0	1	0	1
1	0	1	0
1	1	\overline{Q}	Q



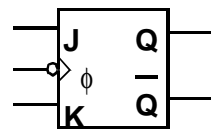
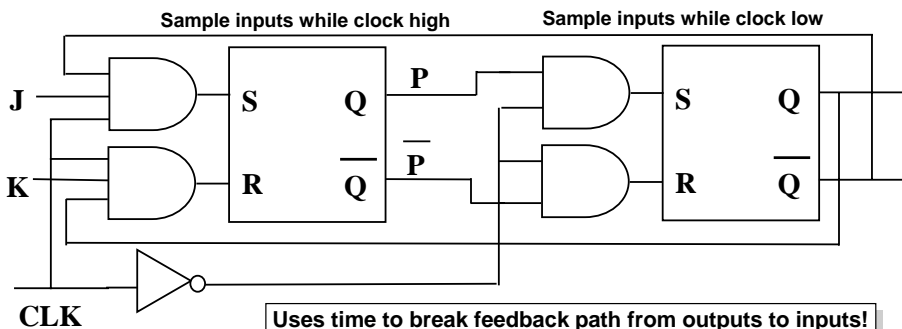
- Eliminate the forbidden state of the SR flip-flop.
- Use output feedback to guarantee that R and S are never both one.

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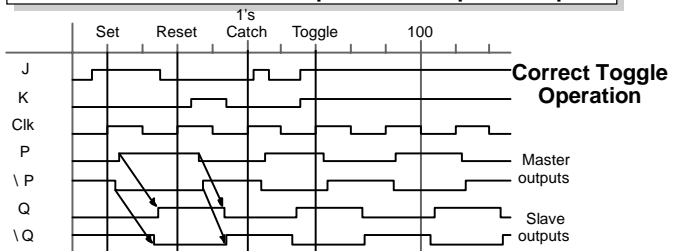
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JK Master-Slave Register



JK Logic Symbol

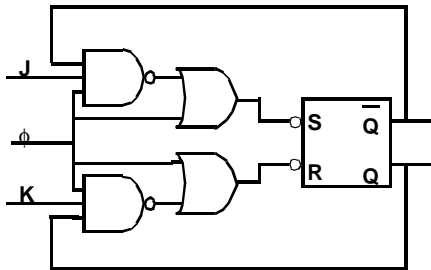
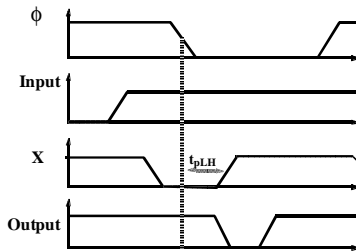
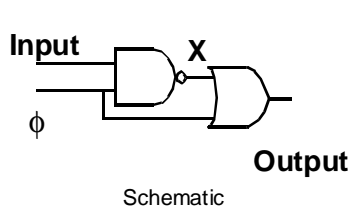


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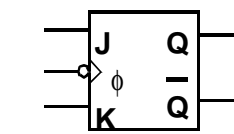
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Pulse Based Edge-Triggered JK Register



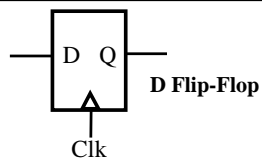
JK Register Schematic



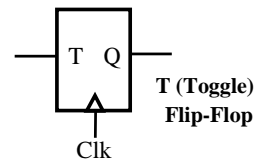
JK Register Logic Symbol



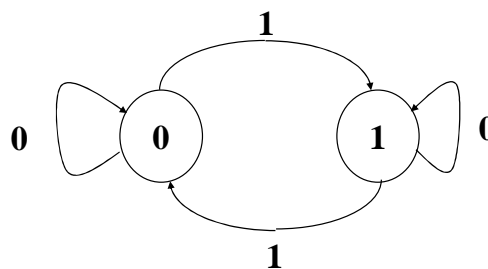
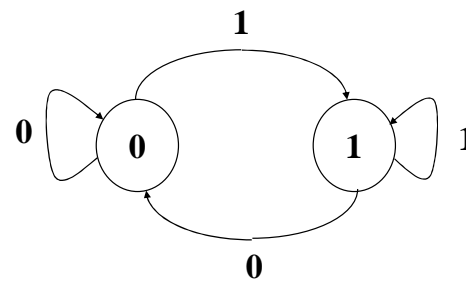
D Flip-Flop vs. Toggle Flip-Flop



D	Q_N
0	0
1	1



T	Q_N
0	Q_{N-1}
1	\bar{Q}_{N-1}





Realizing Different Types of Memory Elements



Characteristic Equations

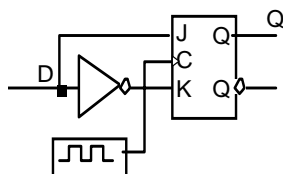
$$D: Q^+ = D$$

$$JK: Q^+ = J\bar{Q} + \bar{K}Q$$

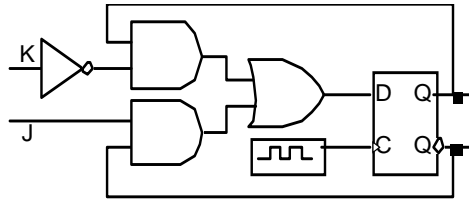
$$T: Q^+ = T\bar{Q} + \bar{T}Q$$

E.g., $J=K=0$, then $Q^+ = Q$
 $J=1, K=0$, then $Q^+ = 1$
 $J=0, K=1$, then $Q^+ = \bar{Q}$
 $J=1, K=1$, then $Q^+ = \bar{Q}$

Implementing One FF in Terms of Another



D implemented with JK



JK implemented with D



Design Procedure



Excitation Tables: What are the necessary inputs to cause a particular kind of change in state?

Q	Q ⁺	J	K	T	D
0	0	0	X	0	0
0	1	1	X	1	1
1	0	X	1	1	0
1	1	X	0	0	1

Implementing D FF with a J-K FF:

- 1) Start with K-map of $Q^+ = f(D, Q)$
- 2) Create K-maps for J and K with same inputs (D, Q)
- 3) Fill in K-maps with appropriate values for J and K to cause the same state changes as in the original K-map

		D	
		0	1
Q	0	0	1
	1	0	1

$Q^+ = D$

E.g., $D = Q = 0, Q^+ = 0$
then $J = 0, K = X$

		D	
		0	1
Q	0	0	1
	1	X	X

$J = D$

		D	
		0	1
Q	0	X	X
	1	1	0

$K = \bar{D}$



Design Procedure (cont.)



Implementing JK FF with a D FF:

1) K-Map of $Q^+ = F(J, K, Q)$

2,3) Revised K-map using D's excitation table

It's the same! That is why design procedure with D FF is simple!

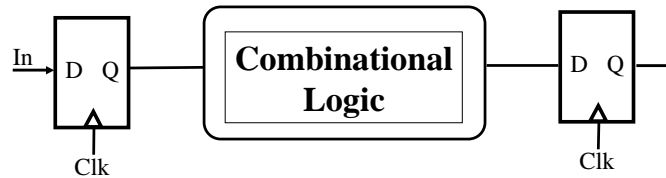
		J			
		00	01	11	10
Q	0	0	0	1	1
	1	1	0	0	1
		K			

$$Q^+ = D = J\bar{Q} + \bar{K}Q$$

Resulting equation is the combinational logic input to D to cause same behavior as JK FF. Of course, it is identical to the characteristic equation for a JK FF.



System Timing Parameters



Register Timing Parameters

T_{cq} : worst case rising edge
clock to q delay

$T_{cq,cd}$: contamination or
minimum delay from
clock to q

T_{su} : setup time

T_h : hold time

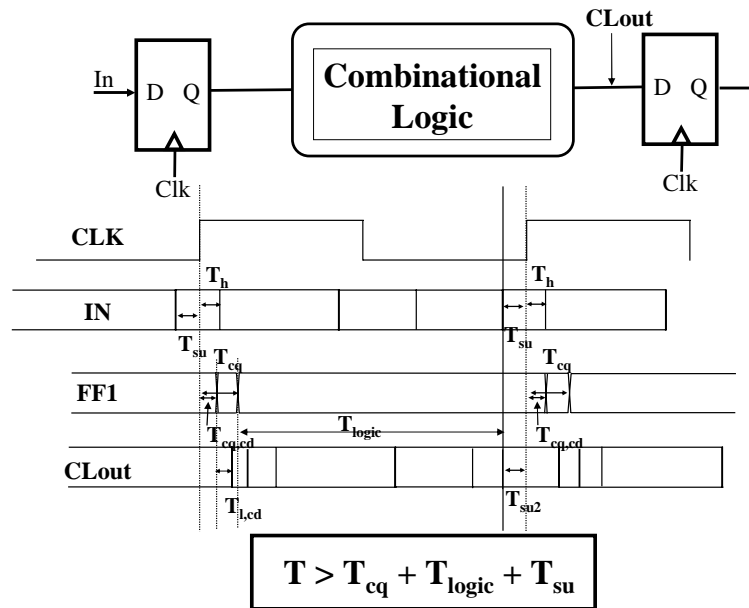
Logic Timing Parameters

T_{logic} : worst case delay
through the combinational
logic network

$T_{logic,cd}$: contamination or
minimum delay
through logic network



System Timing (I): Minimum Period

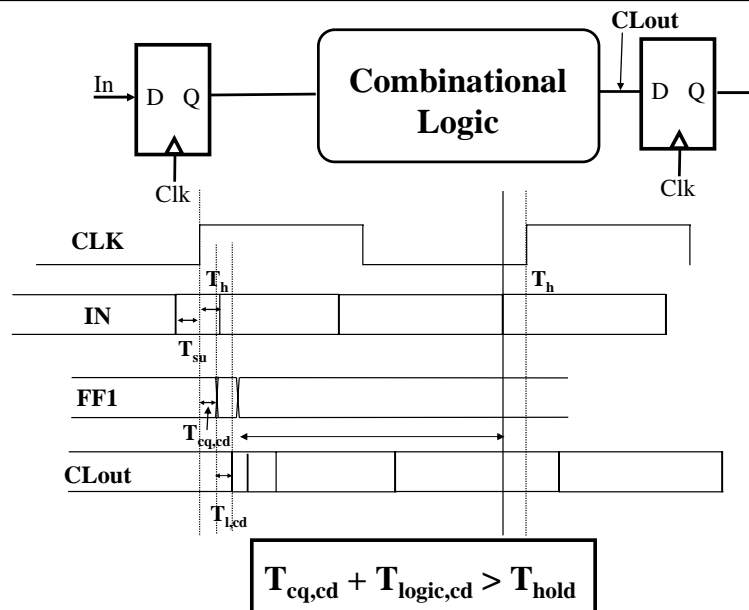


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System Timing (II): Minimum Delay



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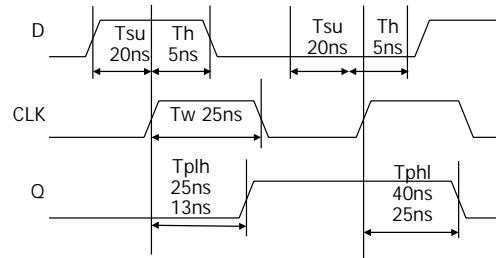
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Shift Register

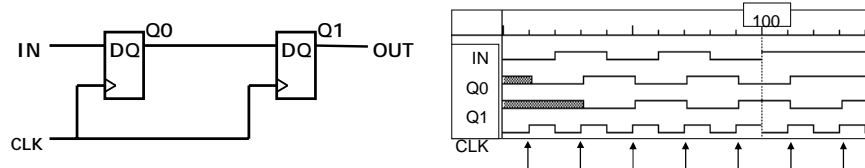


■ Typical parameters for positive edge-triggered D Register



All measurements are made from the clocking event, that is, the rising edge of the clock.

■ Shift register



Clocks are Not Perfect: Clock Skew

