

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 Introductory Digital Systems Laboratory, Fall 2003

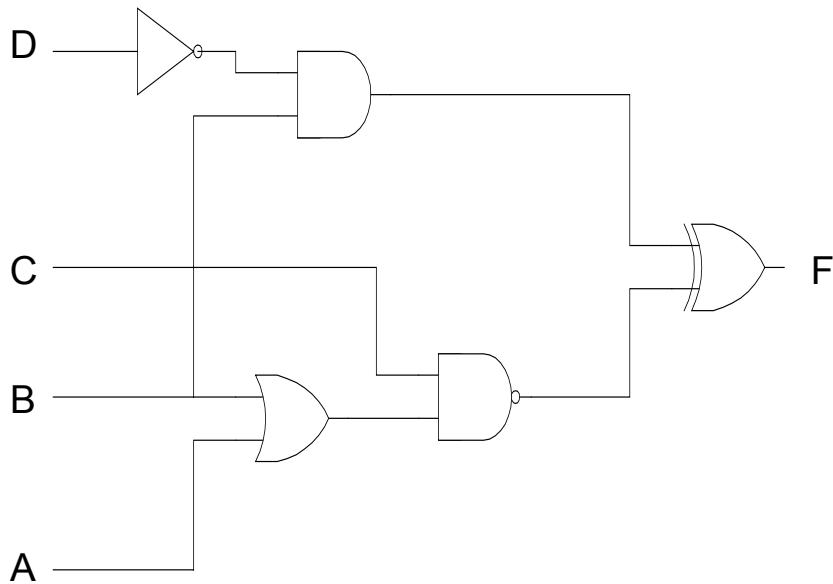
Problem Set 2

Issued: September 10, 2003

Due: September 17, 2003 (No Class – hand in on 9/19)

Problem 1: Combinational Logic

- (a) Derive the logic equation for output F as a function of the inputs A, B, C, D expressed in sum of product form. This expression need not be minimal.



- (b) Build a truth table for the output F.
 (c) Draw the Karnaugh map for the circuit. Circle appropriate groups to find the minimal sum of products and write the expression.
 (d) Is the MSP expression free from static hazards? If so indicate where they occur on the K-map and show how would you remove them or if not, why not?
 (e) Write a VHDL file that implements the function F. Compile and simulate it using the Max+plus II software. Include a printout of your code and a screenshot of the simulation.

Problem 2: Counters

- (a) The 74LS163 is a synchronous counter while the 74LS393 is a ripple counter. Comment on the differences between these two in terms of how they might be used in a design and their performance.
 (b) There are two enable inputs /ENT and /ENP on these counters. How are they different?

- (c) Harvard University has hired you to design a counter to track the number of students entering and exiting a computer lab. This lab can hold a maximum of 30 students. A sensor provides two inputs: enter - pulses when 1 person enters, and exit - pulses when 1 person leaves. Your system should provide a running count of the number of students at any given time as well as a warning signal (FULL) when the maximum is reached. Assume once the max is reached no one else is allowed to enter. Design a counter circuit to implement this system and show a wiring diagram of your circuit.

Problem 3: Flip-Flops

Using the timing diagram below, draw the output of Q for a positive edge-triggered T flip-flop, positive edge-triggered D flip-flop, and a positive edge-triggered JK flip-flop. Assume that Q starts as a 0. Turn in this diagram with your solution.

