

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 - Introductory Digital Systems Laboratory

Created 09/20/99 by D. Seth
Revised 12/17/99 by D. Troxel

CPLD MODULE

The CPLD module comprises of four interconnected Cypress 374I CPLD's that can be accessed via the kit's NuBus interface and 50-pin connectors. The state of the I/O lines of the NuBus interconnects are displayed on the HEX LED's while the I/O lines of the 50 pin connector extend directly to the inputs of the Logic Analyzer.

The diagram below shows the architecture of the module and its interface to the kit.

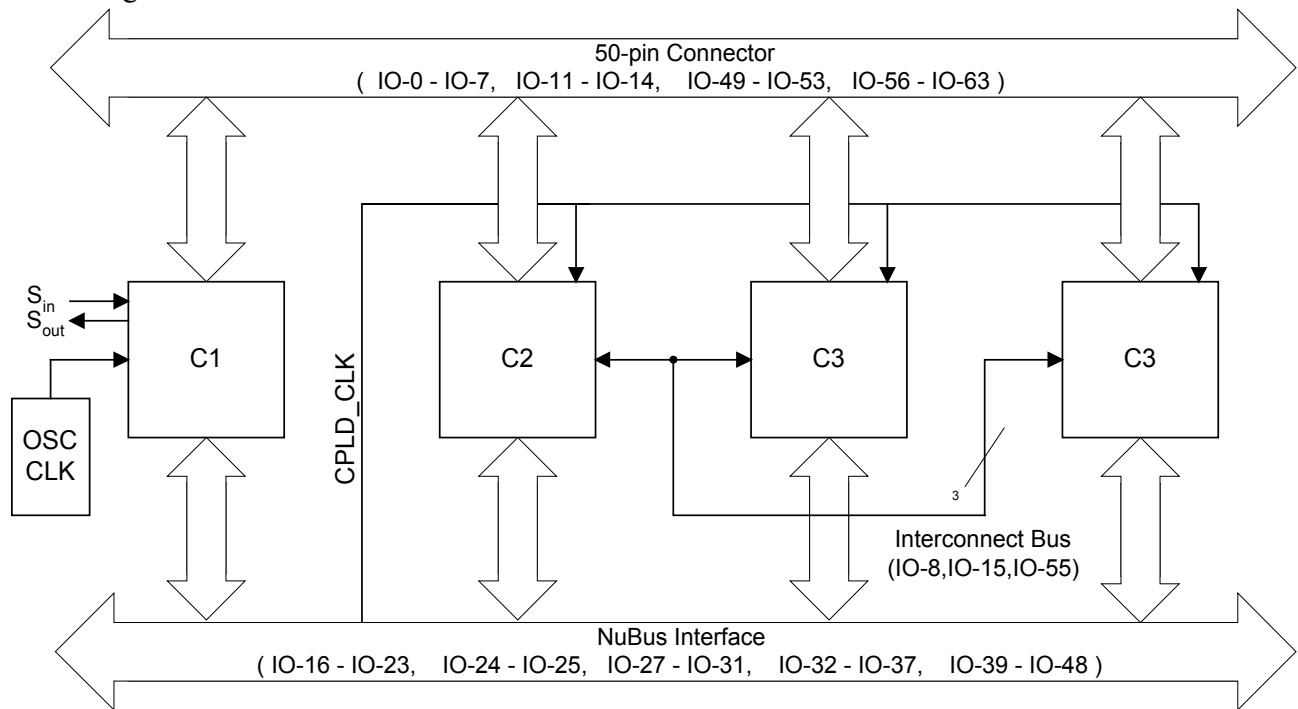


Figure 1: System Diagram

The major components of the module can be categorized into the NuBus Interface, the 50-pin connector Interface, the Interconnect Bus, the Serial Interface, the Programming Interface and the Clocking Scheme.

NuBus Interface

31 I/O pins of each CPLD are interconnected and extended to the NuBus connector. For example, IO-0 of all 4 CPLD's are tied together to NuBus Address A0. Table 1 elaborates these interconnections.

Table 1 : NuBus Interface

| NuBus Address | CPLD(1,2,3,4) I/O Designation | CPLD Pin Designation | Logic Block |
|----------------------|--------------------------------------|-----------------------------|--------------------|
| A0 | IO-16 | 24 | C |
| A1 | IO-17 | 25 | C |
| A2 | IO-18 | 26 | C |
| A3 | IO-19 | 27 | C |
| A4 | IO-20 | 28 | C |
| A5 | IO-21 | 29 | C |
| A6 | IO-22 | 30 | C |
| A7 | IO-23 | 31 | C |
| A8 | IO-24 | 33 | D |
| A9 | IO-25 | 34 | D |
| A10 | IO-27 | 36 | D |
| A11 | IO-28 | 37 | D |
| A12 | IO-29 | 38 | D |
| A13 | IO-30 | 39 | D |
| A14 | IO-31 | 40 | D |
| A15 | IO-32 | 45 | E |
| A16 | IO-33 | 46 | E |
| A17 | IO-34 | 47 | E |
| A18 | IO-35 | 48 | E |
| A19 | IO-36 | 49 | E |
| A20 | IO-37 | 50 | E |
| A21 | IO-39 | 52 | E |
| A22 | IO-40 | 54 | F |
| A23 | IO-41 | 55 | F |
| A24 | IO-42 | 56 | F |
| A25 | IO-43 | 57 | F |
| A26 | IO-44 | 58 | F |
| A27 | IO-45 | 59 | F |
| A28 | IO-46 | 60 | F |
| A29 | IO-47 | 61 | F |
| A30 | IO-48 | 66 | G |
| A31 | See Clock Interface | | |

50-Pin Connector Interface

25 I/O pins are interconnected among the 4 CPLD's and the 50-pin connector. The signals of the 50-pin connector interface directly to the logic analyzer via the connector on the kit.

Table 2 provides details of these interconnections. Logic Blocks are partitions internal to the CPLD chip. This information, at times, can be useful during device fitting.

Table 2: 50-pin Connector Interface

| CPLD I/O | CPLD PIN | LOGIC BLOCK | 50-PIN PIN # (KIT) | K1 INTERFACE | K2 INTERFACE |
|----------|----------|-------------|--------------------|--------------|--------------|
| IO-0 | 3 | A | 49 | L1-0 | L2-8 |
| IO-1 | 4 | A | 47 | L1-1 | L2-9 |
| IO-2 | 5 | A | 45 | L1-2 | L2-10 |
| IO-3 | 6 | A | 43 | L1-3 | L2-11 |
| IO-4 | 7 | A | 41 | L1-4 | L2-12 |
| IO-5 | 8 | A | 39 | L1-5 | L2-13 |
| IO-6 | 9 | A | 37 | L1-6 | L2-14 |
| IO-7 | 10 | A | 35 | L1-7 | L2-15 |
| IO-11 | 15 | B | 33 | L1-8 | GND |
| IO-12 | 16 | B | 31 | L1-9 | L3-0 |
| IO-13 | 17 | B | 29 | L1-10 | L3-1 |
| IO-14 | 18 | B | 27 | L1-11 | L3-2 |
| IO-49 | 67 | G | 25 | L1-12 | L3-3 |
| IO-50 | 68 | G | 23 | L1-13 | L3-4 |
| IO-51 | 69 | G | 21 | L1-14 | L3-5 |
| IO-52 | 70 | G | 19 | L1-15 | L3-6 |
| IO-53 | 71 | G | 17 | GND | L3-7 |
| IO-56 | 75 | H | 15 | L2-0 | L3-8 |
| IO-57 | 76 | H | 13 | L2-1 | L3-9 |
| IO-58 | 77 | H | 11 | L2-2 | L3-10 |
| IO-59 | 78 | H | 9 | L2-3 | L3-11 |
| IO-60 | 79 | H | 7 | L2-4 | L3-12 |
| IO-61 | 80 | H | 5 | L2-5 | L3-13 |
| IO-62 | 81 | H | 3 | L2-6 | L3-14 |
| IO-63 | 82 | H | 1 | L2-7 | L3-15 |

Note: If you use K1, then IO-53 must not be used. Similarly, if you use K2, then IO-11 must not be used.

Serial Interface

The CPLD Module supports an RS-232 interface via the DB-9 Male connector. The received serial data from Pin 2 of the DB-9 is brought to logic levels via inversion from a MAX 233 and is made available on Pin 12 of CPLD 1. The data to be transmitted is presented at Pin 73 of CPLD 1, which appears on Pin 3 of the DB-9 after being inverted by the MAX 233. Please see [/mit/6.111/vhdl/serial/](#) for VHDL code that emulates a receiver and a transmitter.

Clock Interface

The figure below presents the clocking scheme used by the module.

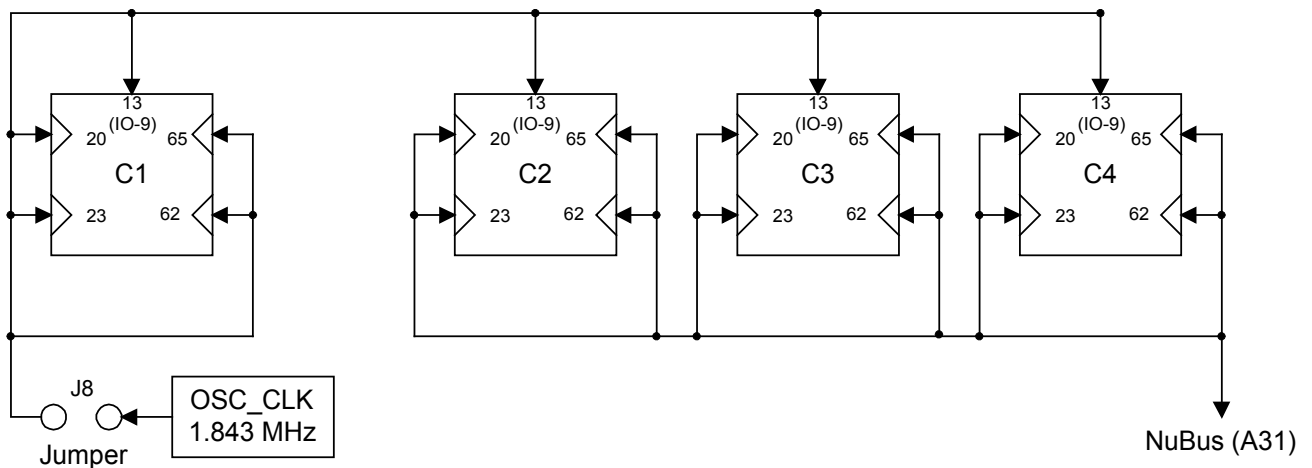


Figure 2 : Clocking Scheme

The following are some clocking strategies that can be utilized:

- 1) C1 sources its clock from the oscillator by enabling jumper J8, while C [2,3 or 4] can buffer this signal (IO-9) to any connection on the NuBus, e.g. A30. A short circuit can then be created between this interconnection, i.e. A30 and A31 by installing a jumper wire.
- 2) C [2,3 or 4] buffer A31 to IO-9 thereby clocking C1. In this scenario, jumper J8 is removed and an external clock is supplied to A31.
- 3) Jumper J8's strategic location makes it possible to insert a wire within the jumper and plug the other end into NuBus A31. If this is done, a termination resistor (discussed ahead) may be required between A31 and GND located on the NUBus connector.
- 4) Make C1 use a separate clock, while C [2,3, and 4] share their clock from A31.

Irrespective of the clocking strategy, it is always important to consider the effects of clock skew.

Interconnect Bus

A 3-bit bus exists between CPLD 2, 3, and 4. This bus does not have an external interface, i.e. it cannot be accessed via the NuBus or the 50-pin connector interface. The details of these interconnections are:

| CPLD I/O [C2,C3 and C4 only] | CPLD Pin | Logic Block |
|---------------------------------|----------|-------------|
| IO-8 | 12 | B |
| IO-15 | 19 | B |
| IO-55 | 73 | G |

Programming

The module supports the In-System Re-Programming of CPLD's. The following steps are the programming procedure:

- 1) Disable **all** clocks to **all** CPLD's. Cypress admits to a bug in the 374I CPLD in which the programming is incorrect if the input clock is running. This means removing jumper J8 and the input to A31. This also applies to the CPLD's not being programmed. For instance, if you want to program CPLD # 2 only, Jumper J8 must be removed to avoid corrupting CPLD #1. All CPLDs are supplied with +12V when any CPLD is programmed.
- 2) Insert the 10-pin ribbon connector from the programmer into the blue 10-pin socket. The **right orientation is critical - check the key along with the diagrams in the lab.**
- 3) Select the proper jumper configuration from the table below. A '1' means connected while a blank signifies 'open'.

Table 3 : Jumper Selections

| Description | C4 | C3 | C2 | C1 | J1 | J2 | J3 | J4 | J5 | J6 | J7 |
|-------------|----|----|----|----|----|----|----|----|----|----|----|
| C1 only | | | | 1 | 1 | | | | | | |
| C2 only | | | 1 | | | 1 | 1 | | | | |
| C3 only | | 1 | | | | | | 1 | 1 | | |
| C4 only | 1 | | | | | | | | | 1 | 1 |
| C1,C2 | | | | | | | 1 | | | | |
| C1,C2,C3 | | | | | | | | | 1 | | |
| C1,C2,C3,C4 | 1 | 1 | 1 | 1 | | | | | | | 1 |

- 4) Choose one of the following programming routines :
 - "4cpld374 config.file" to program/bypass/erase all the CPLDs. "4cpld374 -help" provides details on the configuration file specifications. We expect you to use this programming routine. As Table 3 suggests, only Jumper J7 must be in place.

- "cpld374 file.jed" to program only one CPLD. The Jumper settings can be found in Table 3.
 - "3cpld374 config.file" to program/bypass/erase the first three CPLDs.
 - "2cpld374 config.file" to program/bypass/erase the first two CPLDs.
- 5) The programmer then referring to switch SW1 asks that it be pulled backward. Upon moving SW1 in the backward position, the green LED turns off and the red LED turns on. At this stage, the programmer also mentions the files that will be loaded onto the respective CPLD's. It is a good idea to verify this, by observing the list displayed on the screen.
 - 6) The selected CPLD's are then programmed and a "Successful" is returned if all goes well. It is essential to verify that the programming was "Successful".
 - 7) Push SW1 forward to enable the green LED.

If there appears to be problems with the programmer, refer to the CPLD startup procedure on 6.111 Homepage or consult a TA.

Test Programs

We have two programs to test the board. They are intended to verify the operation of the CPLD as well as the connections between the 50-pin connector and the logic analyzer.

- **Driver** : This program loads a 31 bit counter that is displayed on the NuBus LED's.
- **Reader**: This program reads the first 25 I/O lines of the NuBus connector and extends them to the 50-pin connector .

The output of the first 25 bits of the NuBus can therefore be seen on the Logic Analyzer. The remaining 6 bits on the NuBus can be directly probed by the scope.

The above files along with an empty pre-numbered VHDL file (374sample.vhd) can be found at [/mit/6.111/cpld/sources/](#) .

Termination

The diagram below shows a high frequency square wave when observed with an analog scope :

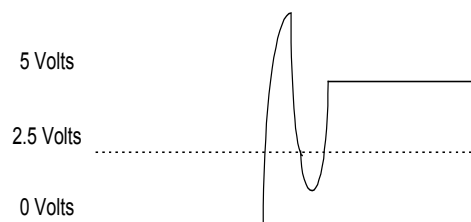


Figure 3 : Ringing

Clearly, if this signal were to be a clock-input to a device, there would be some serious problems. All signals used as clocks must be verified to see if termination is necessary. Inserting a resistor on the proto-board between the signal and ground can reduce this swing. A 100 Ω resistor is ideal for most cases.

Note that with a 100 Ω termination, the signal's logic high is now about 3.8 Volt, which satisfies the requirements of a TTL compatible device. If you feel the need to terminate a bus, ask the front desk for a resistor network. Its logic diagram is as follows:

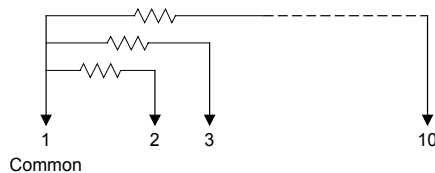
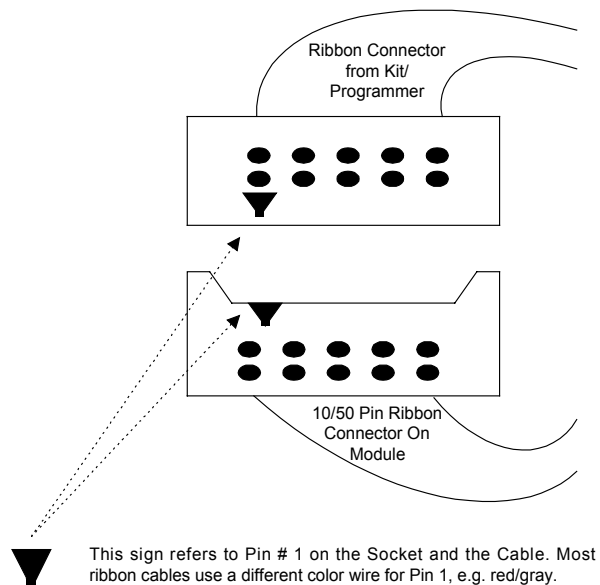


Figure 4 : Resistor Network

Common Errors

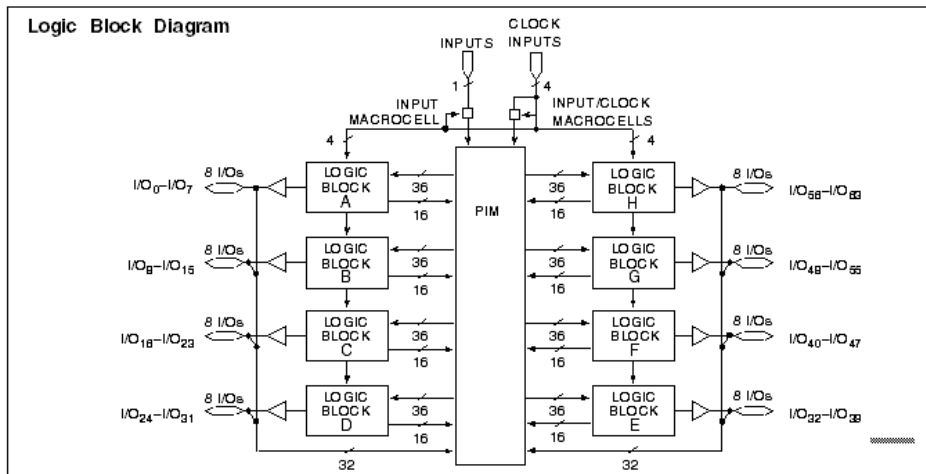
- If you use K1 of the kit to interface with the module, then IO-53 must not be used. Similarly, if K2 is used, then IO-11 must not be used. Refer to Table 2, which lists these pins as 'GND'.
- The 50-pin connector and the programming 10-pin connector must be inserted in the right way. The diagram below explains the proper alignment of Pin 1.



- All clocks must be disabled before commencing programming.
- Critical signals such as clock sources may require termination. Verify this with an analog scope.
- Don't forget to push SW1 forward upon the completion of programming.

About the Cypress CYC374I CPLD

The 128 macrocells in the 84 pin CY7C374i are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator. You can refer to <http://www.cypress.com/pub/datasheets/pld/cy7c374i.pdf> for more details.



The pin layout of the CYC374I CPLD is

