

Massachusetts Institute of Technology
 Department of Electrical Engineering and Computer Science
 6.111 – Introductory Digital Systems Laboratory

Problem Set 2

Issued: February 9, 2000

Due: February 16, 2000

Problem 1: Don't You Love Combinational Logic?

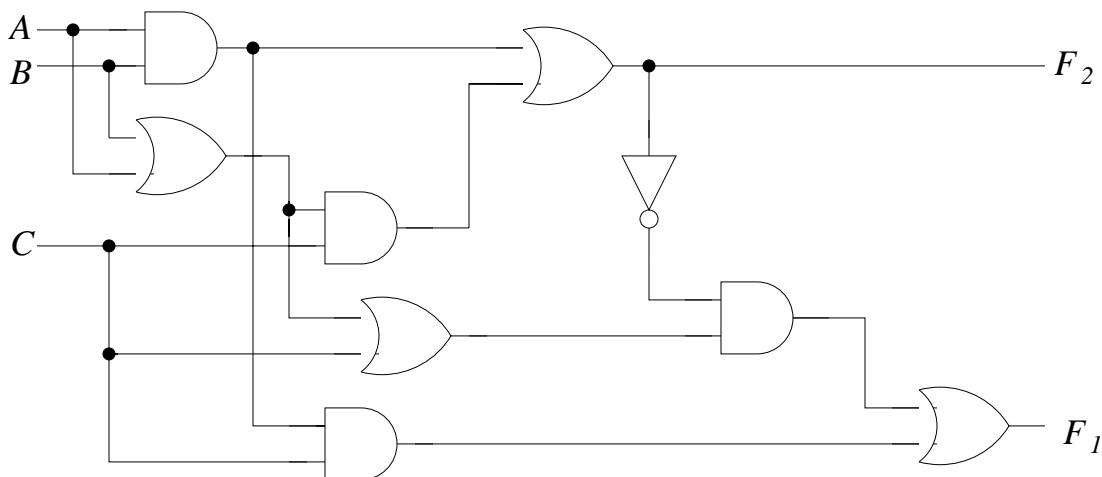


Figure 1: The above circuit.

1. Derive the truth table of the above circuit. Can you explain what its function is?

(option)

2. Find the MSP and MPS expressions for function F_2 using a Karnaugh map, and circle the appropriate groupings. Draw the circuit diagram for each implementation, using only '04, '08, and '32 chips that can be found in your lab kits. Which form can be wired using fewer gates? Assuming each gate has a delay of 5 ns, which form of logic propagates faster?

Bonus: Why weren't you asked to try to reduce F_1 to MSP or MPS? What additional kinds of gates might help you simplify the circuit for F_1 ? (Hint: Look at the truth table)

(option)

3. If you were able to also use '10 and '20 gates, could you construct either the MSP or MPS circuit with fewer gates?

4. Now, using the '151 multiplexer, implement function F_1 . (Hint: Consider the address pins as the input variables, and the eight channels as values to be selected.)

(option)

5. Suppose you only had a 4:1 multiplexer. Can you still implement the function F_1 ?

Problem 2: Digital Waffling

Using the following timing diagram, draw the output Q (assuming Q starts at 1) for a positive-edge-triggered D flip-flop, a negative-edge-triggered T flip-flop, and a negative-edge-triggered JK flip-flop.

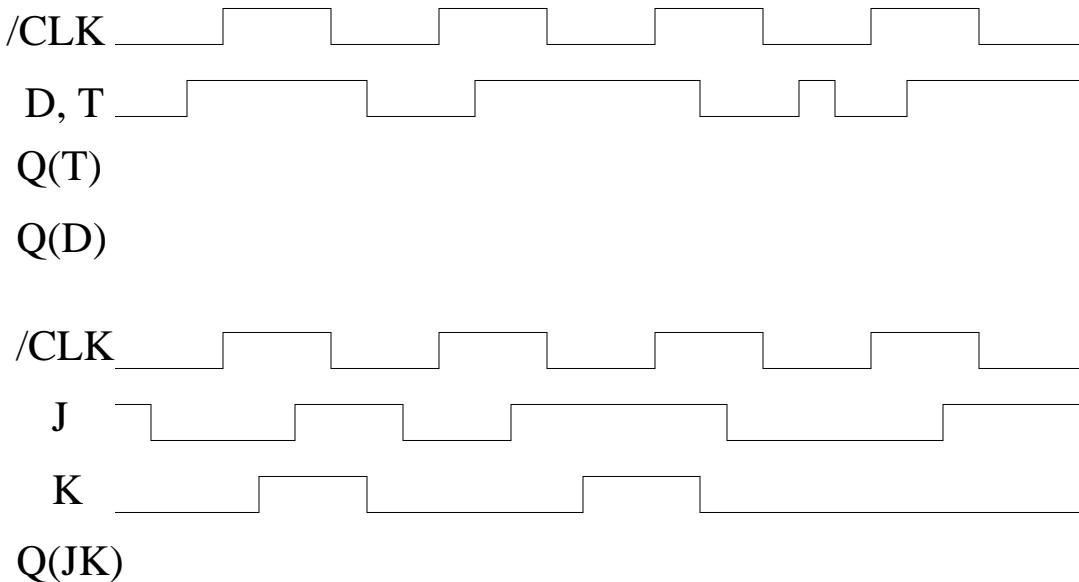


Figure 2: Flip flop timing diagram.

Problem 3: Fun with Counters

1. The '393 is called a ripple counter, while the others are synchronous. What does this mean? What is the difference?
2. $\overline{/ENT}$ and $\overline{/ENP}$ on the counters are not the same. What is the difference?
3. You are a ticket taker at the county fair, and you've been using that mechanical people counter thingy for your entire illustrious career. Now that you are taking 6.111, you decide it's time for some technological advancement. The fairgrounds have room for 33 people at a time (Boston kids don't tend to sign up for the 4-H club) and you are responsible for making sure too many people aren't inside at once.

So you must design a counter circuit which indicates when 33 people have entered the fairgrounds. It needs an input that you would press each time a person enters, and it should have an output indicating when the fair is full. There should also be an input so that when someone leaves, you can decrement the count of people. You can use whatever counter chips are in your lab kit (although one certain counter chip would be particularly suitable), plus any gates needed for auxiliary combinational logic.

(option)

4. You probably don't want to lug your nerd kit all the way to your part-time job, so it would be better to have all this circuitry in a single CPLD, so that you can have a sleek handheld device instead. Design the above circuit in VHDL.