1.1 GOAL 6.111 S2001

Wednesday, February 7, 2001

Design and Implement Complex Digital Systems.

- Use a Hardware Design Language (VHDL).
- Implement with Multiple Existing Integrated Circuits.
- Prior Digital Design Experience is not Necessary.
- Prequisite is Something to do with Circuit Theory.
- 6.004 is NOT a Prerequisite.
  - Take 6.004 before 6.111 or
  - Take 6.004 after 6.111 or
  - Take both in the same term

1.2 APPROACH

- Knowledge
  - Theory
  - Examples
  - Design rules
  - Guidelines
  - Instruction
- Environment
  - Lab space
  - Oscilloscopes
  - Logic Analyzers
  - Way to build things
  - Programming equipment
  - Computers
  - Design software

1.3 Challenges

- Start with structured assignments and structured solutions.
  - Problem Sets, Lab 1, and Quizzes
- Next are structured assignments with unstructured solutions.
  - Lab 2 and Lab 3
- Finally we have an unstructured assignment and unstructured solution.
  - Project
- We the teaching staff, provide HELP with debugging and testing, ENCOURAGEMENT, and liberal PRAISE as success evolves.

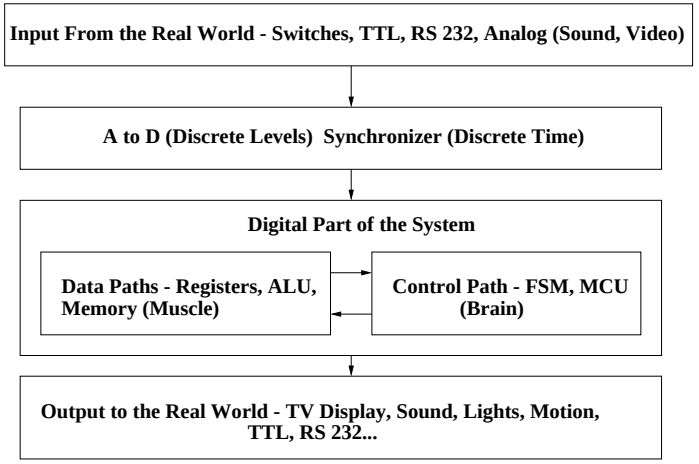
1.4 Grading and Honesty

- We start with a number and then discuss everyone, especially performance in labs and project.
  - **Quizzes (20%)**
  - **Problem sets (10%)**
  - **Lab exercises (35%)**
  - **Project (35%)**
  - **As you see, this is primarily a lab course.**
- Cooperation
  - Do not collaborate with anyone on quizzes.
  - Collaborate with anyone on problem sets and labs and then do them individually.
  - Collaborate with anyone on the project and do the project cooperatively with your project partners.

1.5 Labs

- Lab 1
  - Find the lab and wire something.
  - Program and test a PAL.
  - Learn how to use an oscilloscope and a logic analyzer.
- Lab 2
  - Design and implement a (quite complicated) Finite State Machine (FSM).
  - At least part of the design must be in VHDL and use a CPLD (Complex PLD).
- Lab 3
  - Design and implement a (quite complicated) microprogrammed system.
  - Use VHDL to program CPLDs and PALs.
  - Lab 3 is a good prototype for the size and complexity of each individual's part of the final project.

1.6 DIGITAL SYSTEMS



1.7 VHDL

VHSIC Hardware Description Language

- Language to express digital systems
  - Structural
  - Behavioral
  - Timing
- Rich and powerful language
- Basic standard environment
- Supports both
  - Hardware concepts
  - Software concepts

1.8 VHDL Example

```
-- Massachusetts (Obsolete) Stoplight Example
library ieee;
use ieee.std_logic_1164.all;
entity check is port(
        r, y, g:        in std_logic;
        ok: out std_logic;
        signal t1, t2, t3: inout std_logic);
end check;
architecture logical of check is
begin
        my_label: process(r, y, g, t1, t2, t3) begin
                t1 <= r and (not g);
                t2 <= y and (not g);
                t3 <= (not r) and (not y) and g;
                ok <= t1 or t2 or t3;
        end process;
end logical;
```

1.9 VHDL Advantages

- Shorter design cycle
- Improved design quality
- Vendor and technology independence
- Lower design cost
- Design management
- Simulation of design

1.10 VHDL Disadvantages

- A change of culture
  - Away from schematic-based design
  - Towards language-based synthesis
- Cost of getting started
  - Selecting (and paying for) design tools
- Debugging design problems

1.11 Misconceptions

- Just code it in VHDL and the synthesis tool will design the logic.
- VHDL code that simulates the same way will synthesize to the same set of gates.
- The best style is OBJECT ORIENTED.
  - Depends on the objects (always does)
- Synthesis just can't be as good as a design done by a human!
  - Shades of assembly language vs. a higher level language

1.12 What Can be Synthesized?

- Combinational functions
  - Mux, encoder, decoders
  - Comparator
  - Parity generator
  - Adder, ALU
  - Miscellaneous logic
- Counter based functions
  - Counters
  - MAR, FIFO
- Register and latch functions
- Control logic
  - Sequencers, FSM
  - Synchronizers

1.13 Observations

- VHDL is a programming language.
  - There are many good and bad programs.
- Functionality is important.
  - BUT not enough! Style is important.
- Good design is critical.
- Synthesis is hard.
  - Fitter program takes clues from your VHDL code.
- Decomposition of a large design into smaller, understandable sub-parts is essential.

1.14 Design for Testing

- Design can be fun.
- Testing is work.
- Testing is more important than design.
- Untested designs are rarely good designs.
- Almost all of us make mistakes.
- Testing helps catch mistakes.

1.15 How to Use VHDL

- Design before typing,
  - at least a little!
- Start with a working VHDL file,
  - modify it to do what you want to do.
- Use more than one file.
- Compile files as they are typed in.
  - Don't wait until design is completely entered before compiling and/or fitting the VHDL code.
  - Take one step at a time.

1.16 Lab Hours

- Please be out by the indicated time. Instrument room personnel get paid by the hour. Please do NOT take advantage of them. The usual times are:
- Monday - Friday
  - 9:00 AM to 11:45 PM
- Saturday
  - 12:00 Noon to 5:45 PM
- Sunday
  - 12:00 Noon to 11:45 PM
- Hours for Holidays, Spring Break, etc. will be posted.

1.17 Get Your Computer Account

- Go to the Digital Lab, 38-600.
  - Login with your Athena name and password to sunpal1.mit.edu or sunpal2.mit.edu. This will automatically give you an account on the computers in the digital lab. The sunpal machines are located on the near right side of the lab as you enter the lab.
- To access the software available, it is best to login to a machine in the digital lab.
  - If this is an HP machine, you need to do a kinit and enter your password again, then slogin to an Ultra 5 in the Lab.
  - If this is an Athena Ultra 5, simply do setup (not add) 6.111 and you are all set.
  - If this is an Athena machine, but not an Ultra 5, then do setup 6.111 and slogin to an Athena ultra 5 in the lab.
- If you have trouble, ASK.

1.18 Turn In Your Schedule Sheet

- Extra handouts will be in the filing cabinet in the back left corner of the digital lab - 38-600.
- Recitation Assignments will be posted by Friday on the bulletin board in the digital lab and on the 6.111 web page.
- //http:sunpal2.mit.edu
  - Also linked to the department web page.
- Pick up lab kits starting Thursday at 1 pm.