

14.1 Lab 3 Assignment

Monday, March 12, 2001

This lab is hard!

- Many design decisions are up to you, but you **MUST** use an MCU.
- **BUT** you are not expected to spend spring break doing it.

Issued - Monday, March 12, 2001

MCU Checkoff - Monday, March 19, 2001

Design Checkoff - Wednesday, March 21, 2001

Lab Checkoff - Friday, April 6, 2001

Report Due - Monday, April 9, 2001

Pitch Shifting System

- Digitizes and stores audio frequency input signals.
- Outputs pitch shifted version plus (optionally) original signal.

Simple (crude) Pitch Shift Mechanism

- Uses two buffers, samples at fixed rate and outputs at fixed rate.
- Skips or adds samples to achieve pitch shifting.

Selectable Sampling Rate (e.g., 9.6 and 19.2 kHz)

Adjustable Pitch Shift over a Wide Range

- Use pushbuttons to adjust pitch shift UP and DOWN.

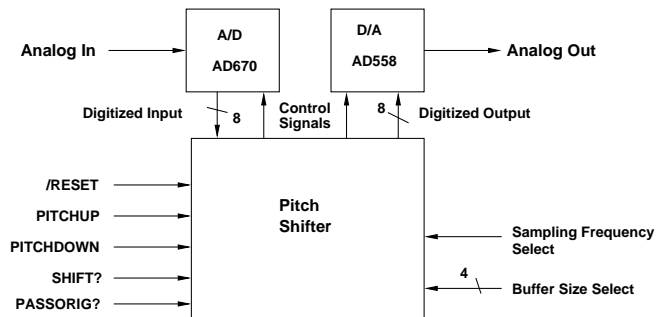
Selectable Buffer Size (16 Buffer Sizes)

14.2 Lab 3: Helium Breath



Analog In Music or speech signal (or a test analog signal)
Analog Out Signal shifted up or down in pitch
/RESET Clear pitch shift to zero
PITCHUP Increments the amount of pitch shift
PITCHDOWN Decrements the amount of pitch shift
SHIFT? When asserted, output pitch shifted audio
PASSORIG? When asserted, output original audio signal
(When both asserted, mix)
Sampling Frequency Select - Choose one of two sampling rates
Buffer Size Select - Choose one of 16 sampling buffer sizes

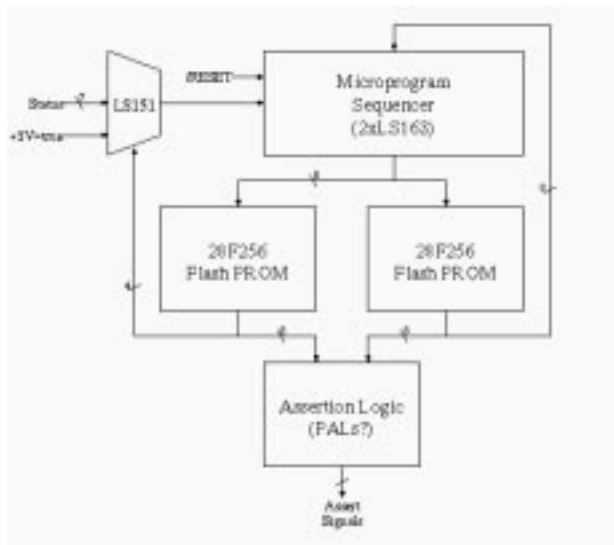
14.3 Analog-Digital Separation



14.4 Approach

- Divide time into 'chunks'.
- Write signal into a buffer (one chunk).
- Use two buffers: write to one while reading from other.
- Output signal at a different rate to change pitch.
 - To lower pitch,
 - 'Stretch' signal in each chunk.
 - This means we throw away end of each chunk.
 - To increase pitch,
 - 'Squish' the signal chunk.
 - Output at a higher rate.
 - To fill the end of the chunk, output some part twice.

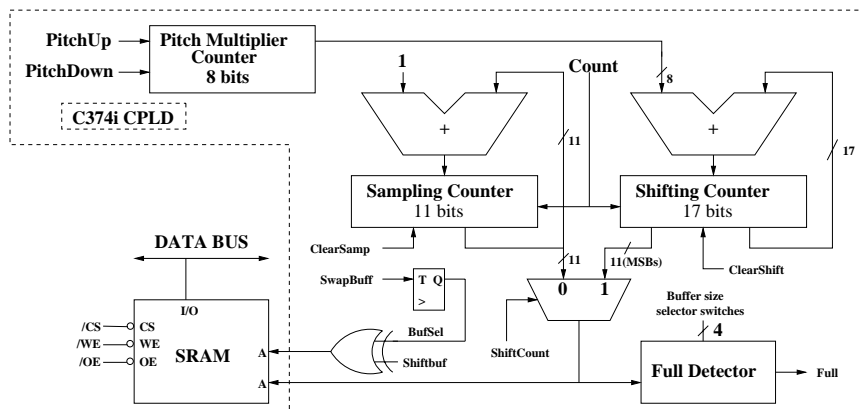
14.9 MCU



14.10 Timing Unit

- Provides MCU Clock.
 - Makes sure timing constraints are observed.
- Provides Sampling Clock.
 - At two rates
- For MCU test yet a lower frequency.
 - 10 to 20 Hz
- Probably should be implemented in a CPLD.

14.11 Storage Unit



14.12 Storage Unit

- SRAM and Memory Address Logic
- Implements Two Storage Buffers
- Switch Address Counters
- Sampling Counter
 - Increments by 1
 - 11 bits => 2K
- Shifting Counter
 - Wider (17 bits => 64 x 2K)
 - Increments by selectable amount
 - Most significant 11 bits skips or repeats
- Switch Buffer
 - MSB of address
 - SwapBuff toggles the buffer.
 - ShiftBuf and ShiftCount to address correct buffer
- Pitch Multiplier Counter
 - Up/Down functions controlled by pushbuttons
- Full Detector
 - With size selector switch
 - To implement variable buffer size

14.13 Signal Accumulator

- To select signals to output
 - Original Input Signal
 - Pitch Shifted Signal
 - Or both added together
- Possible implementation
 - 2 X 74LS283
 - Clearable, loadable, 8-bit register
- You may design another implementation.

14.14 Implementation

- Remember to synchronize asynchronous inputs.
- Pitch Up and Down PB's should produce pulses.
 - One per push or
 - SLOW periodic pulses (if PB held down for a while).
- Do the MCU first and check it out with our program.
- Debug using signal generator.
 - Use sine or triangle waves, NOT voice or music.
- Do signal accumulator last.
- Report requirements are listed in the lab handout.