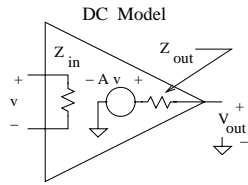


15.1 Operational Amplifiers

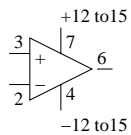
Wednesday, March 14, 2001



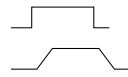
	Ideal	'741	'357
A	∞	$\frac{200,000}{f \text{ (Hz)}}$	$\frac{20 \times 10^6}{f \text{ (Hz)}}$
Z_{out}	0	75 Ohms	
Z_{in}	∞	300 kOhms	10^{12} Ohms

Don't forget to wire the Power Supply!

8-Pin "Mini-Dip



Slew Rate:

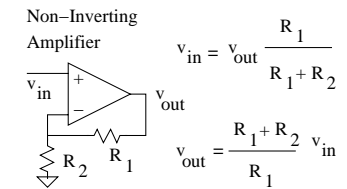
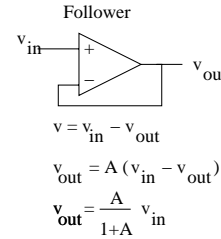


'741: 0.5 V/ μ sec
'357: 50 V/ μ sec

15.2 Uses of Op Amps

□ Analog uses employ negative feedback to drive + input to (nearly) the same potential as the - input.

□ Follower and Non-Inverting Amplifier Circuits:

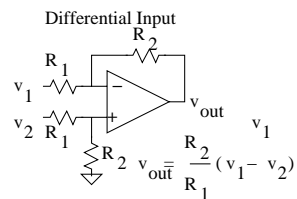
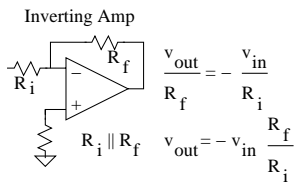


15.3 More Uses of Op Amps

□ Inverting Amplifier and Differential Input Amplifier

□ Resistance seen by the plus and minus inputs should be the same when an op amp is configured for voltage gain.

○ Bias currents (relatively equal) times difference in input resistance look the same as an input signal.

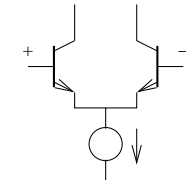


15.4 Bias Currents

□ Many Op Amps have bipolar inputs.

- Emitter coupled transistor pair
- High differential gain
- But sum of input currents = I_e/β .

Input Stage of Op Amp



Op Amps with bipolar inputs stages draw some input (bias) current !

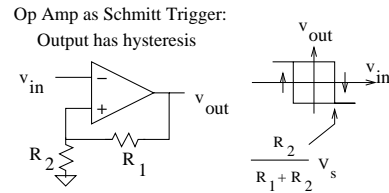
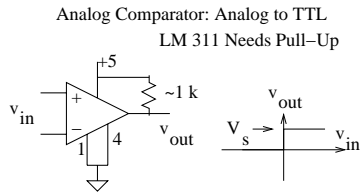
Op Amps with FET inputs stages have very small input (bias) currents.

15.5 Positive Feedback

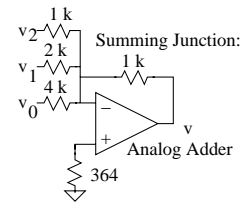
□ Analog Comparator

- Is $V_+ > V_-$?
- Output is a DIGITAL signal.
- The external pull up resistor is often forgotten.

□ Schmitt Trigger squares up signals.



15.6 A to D Converters



If V_+ is at zero potential then so is V_- .
The output voltage is proportional to sum of currents.
Currents are inversely proportional to the resistances
IF the input voltages are the same.

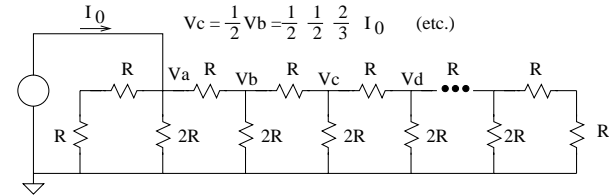
Digital To Analog Converters: Use R - 2R Ladder.

Driving Point Impedance is $2/3 R$.

Voltage Divider Ratio, Node-Node, is $1/2$.

$$V_a = \frac{2}{3} I_0 \quad V_b = \frac{1}{2} V_a = \frac{1}{2} \cdot \frac{2}{3} I_0$$

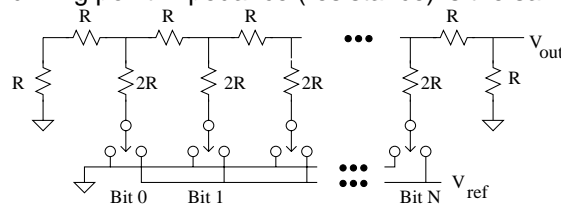
$$V_c = \frac{1}{2} V_b = \frac{1}{2} \cdot \frac{1}{2} \cdot \frac{2}{3} I_0 \quad (\text{etc.})$$



15.7 How to build a D to A

□ Real D to A converters use a voltage reference and switches.

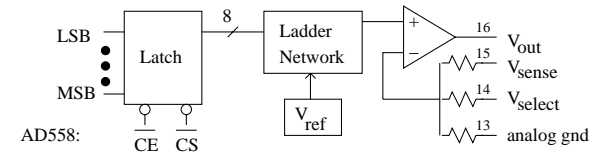
□ Note that the driving point impedance (resistance) is the same for each cell.



$$V_{out} = \frac{1}{6} V_{ref} \left[B_7 + \frac{1}{2} B_6 + \frac{1}{4} B_5 + \dots + \frac{1}{128} B_0 \right]$$

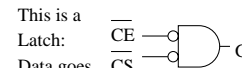
15.8 AD 558

□ 8-Bit D/A Converter you will use in Lab 3.

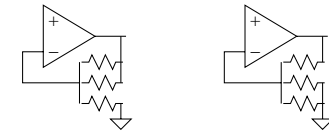


Much like a non-inverting operational amplifier.

Strap Output For Different Voltage:



Output is very noisy when input bits are settling.
It's best to have inputs stable before latching the input data.



0 to 2.5 volts

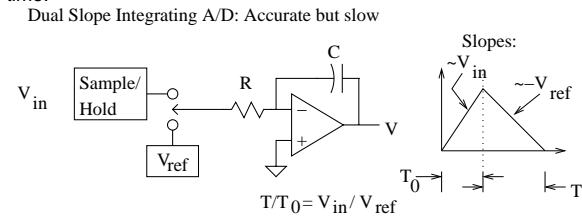
0 to 10 volts
Needs a 12 volt supply!

15.9 Analog to Digital Conversion

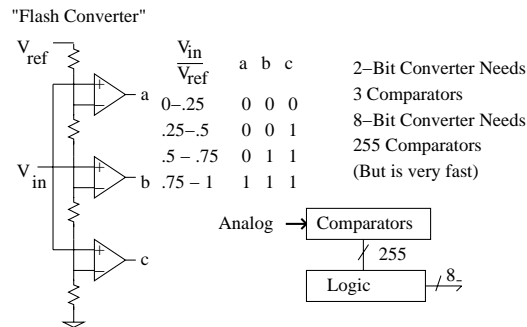
- Harder than Digital to Analog
- Several Different Methods are Used.
- Dual Slope Integration
 - Uses time which can be measured accurately.
 - Typically very accurate but slow.
 - Not widely used any more.
- Multiple Conversions (FLASH)
 - Very fast
 - Used for converting TV signals.
 - Difficult to make in high precision.
 - AD 775
- Successive Approximation
 - Medium speed
 - Can be economical
 - AD 670

15.10 Dual Slope

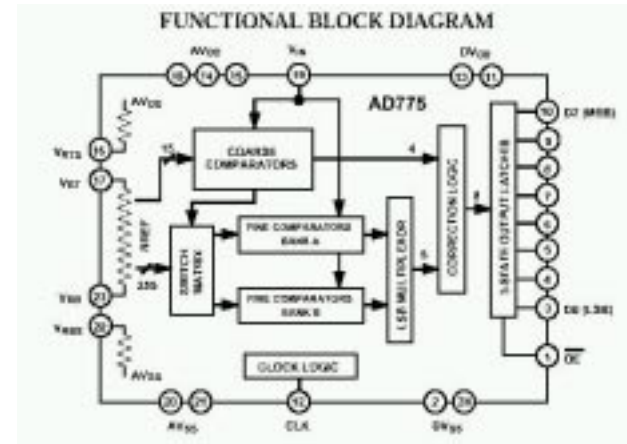
- Dual Slope Integrating A/D
 - Accurate but slow
 - Requires accurate integrator
 - And accurate counter and clock.
- First, Counts for known time
 - with input voltage at input to the integrator.
- Then counts with reference voltage at input
 - and measures time.



15.11 Flash Converter



15.12 AD 775 Functional Block Diagram

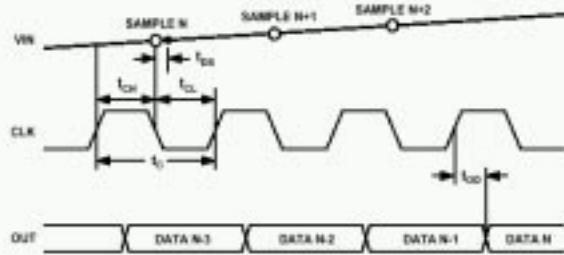


15.13 AD 775 Timing

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate	f_c	20	35		MHz
Clock Period	t_{c1}	50			ns
Clock High	t_{cH}	25			ns
Clock Low	t_{cL}	25			ns
Output Delay	t_{cO}		18	30	ns
Pipeline Delay (Latency)				2.5	Clock C
Sampling Delay	t_{s1}		4		ns
Aperture Jitter			30		ps

Specifications subject to change without notice.



15.14 Voltage Reference

- Similar to other flash converters
 - Needs a stable reference voltage.
 - Can handle different ranges of voltage which
 - is defined by top and bottom of ladder.
- Caution is required: the ladder is fragile!
 - Voltage range is < 2.8 volts.
 - Linearity suffers if < 1.8 volts.
 - AVss means "Analog Voltage" (supply).

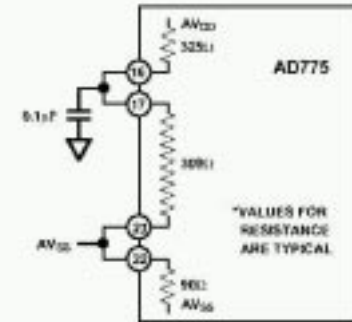
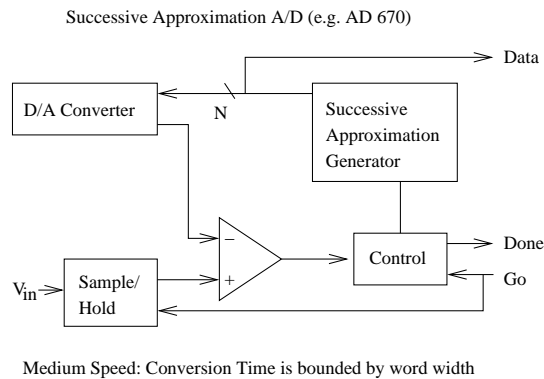


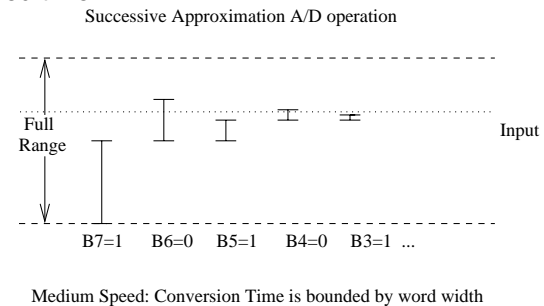
Figure 9. Reference Configuration: 0 V to +2.4 V

15.15 Successive Approximation A/D



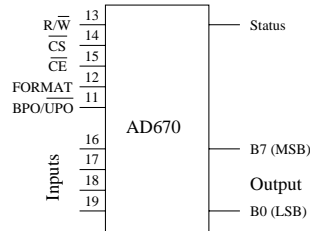
15.16 Operation of Successive Approximation A/D

- Set one bit at a time.
- D/A generates analog voltage.
- Compare with input.
- If overshoot, turn that bit on.
- Finishes in fixed time.



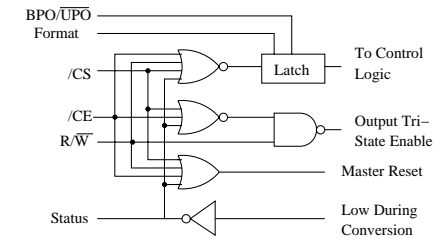
15.17 AD 670

- Conversion time 10 microseconds
- Internal voltage reference
- Multiple input ranges
- Two output formats



15.18 Control Logic for AD 670

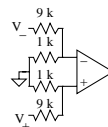
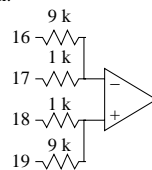
BPO/UPO	Format	Input Range	Output
0	0	Unipolar	Binary
1	0	Bipolar	Binary
0	1	Unipolar	2's Complement
1	1	Bipolar	2's Complement



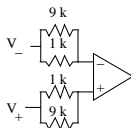
15.19 AD 670 Can Handle Multiple Input Ranges

- High Input Voltage Range
 - Strap Pins 17 and 18 to GND.
- Low Input Voltage Range
 - Strap Pins 16 to 17 and 18 to 19.

Input: Instrumentation Amplifier: strappable
Gain:



High Input Voltage
Connection:
0 to 2.55 V or
-1.28 to +1.28 V

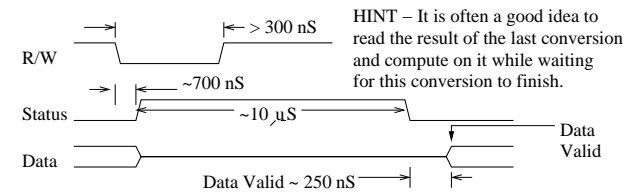


Low Input Voltage
Connection:
0 to 255 mV or
-128 to +128 mV

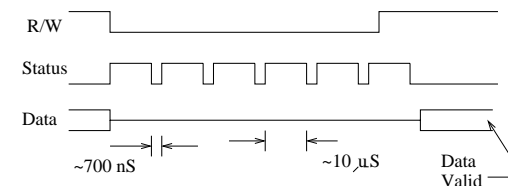
15.20 Timing for AD670

Single Conversion Cycle: Short W valid

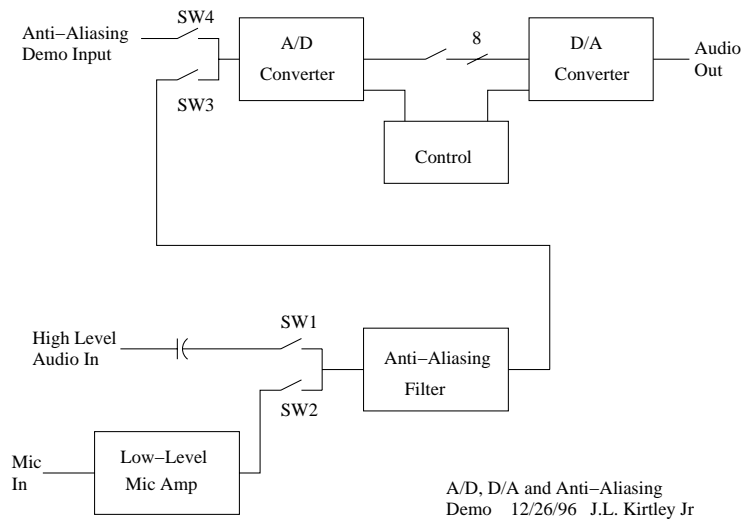
Control bits are /CE, /CS and R/W. Hold R/W low. Must wait for last to finish.
For most uses, tie /CE, /CS to GND. Need to control these if connected to a bus!



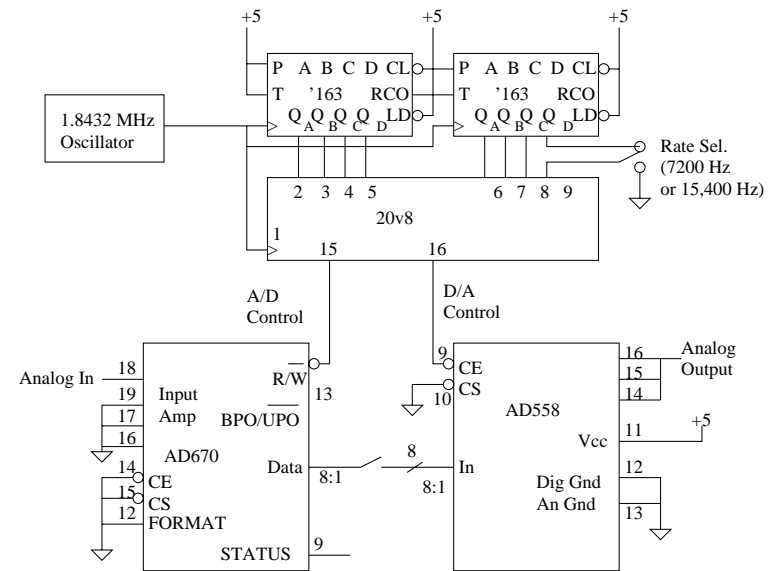
Conversion initiated by R/W LOW pulse



15.21 A/D, D/A and Aliasing Demo



15.22 Control and Digital Section



15.23 Analog: Gain and Anti-Aliasing

