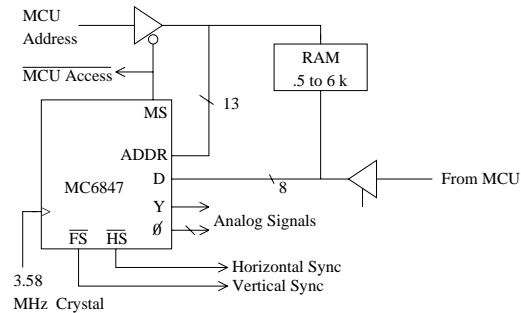


18.0 Video Controllers

From Monday, March 19, 2001

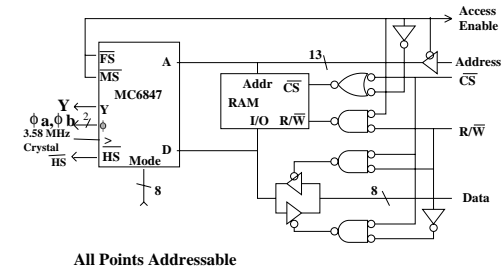
- MC6847 is obsolete but easy to use.
- MC6847 provides a 13-bit address and analog video signal.
- MC6847 reads 8-bit data which can be a character code or video.
- Several display modes include 256 x 192 2 color (well, 1 and black).
- There are other color graphics with lower resolution.



18.1 Bit-Mapped Video

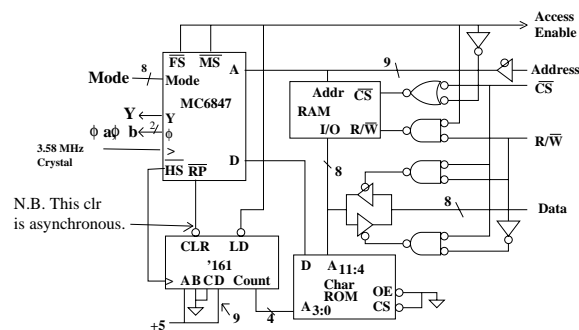
Wednesday, March 21, 2001

- MC6847 display controller
 - Obsolete but useful
- All points addressable
 - Digital system side - more about Y, phi a, and phi b later



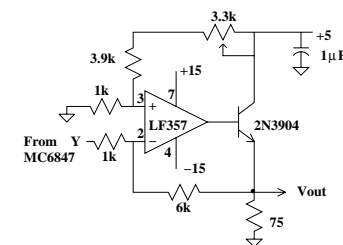
18.2 MC6847 with Character ROM

- You can call it a bug or a feature.
 - To get around the fact that /RP begins and ends between /HS, one must use a '161 which has asynchronous clear.
 - Of course, one could implement the counter with VHDL, but one has to remember to implement an asynchronous clear.



18.3 Black and White (or Green)

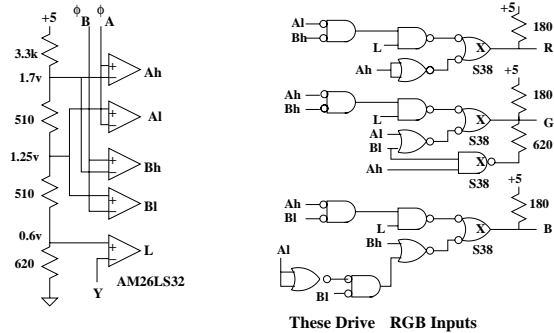
- Simple way of driving a monochrome monitor
 - Has composite sync on the video.
 - Adjust pot (top) so bottom of sync pulse has V=0.



18.4 Color Output

□ Need to decode the 'chroma' outputs.

- The 74S38 driving the 620 ohm resistor is only needed if you want orange.
 - Of course, you can implement this logic with VHDL (in a PAL).
 - N.B. the logic you need depends on the mode used. Look at the Ah, Al, Bh, Bl, and L outputs to determine the logic needed.
- ↳ This logic may not work for the mode you use.



These Drive RGB Inputs

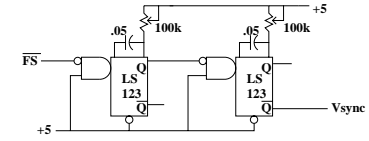
- Comparators on left decode chroma. Gates on right drive RGB.

18.5 Vertical Sync Generation

□ MC6847 generates blanking.

- Here is one legitimate use for one-shots to generate and center sync.

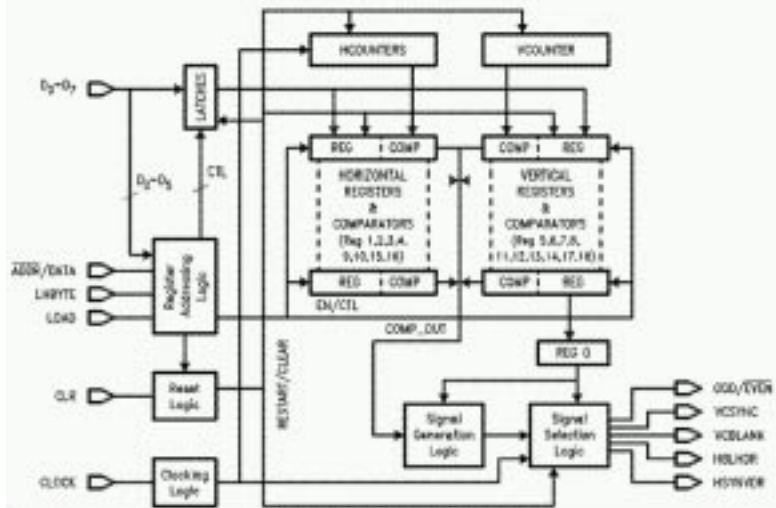
The first one-shot triggers on the falling edge of FS and determines the delay of Vsync. The second one-shot determines the width of Vsync.



RGB Cable

Pin 1	Intensity
Pin 2	Reg
Pin 3	Green
Pin 4	Blue
Pin 5	GND
Pin 6	GND
Pin 7	HSYNC
Pin 8	VSYNC

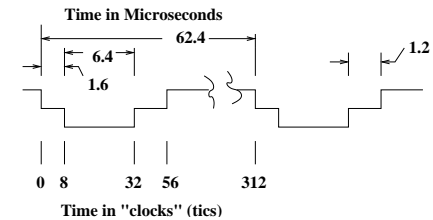
18.6 LM1882 Sync Generator



18.7 Sync Generator Example

□ Flexible, store timing information in registers.

- See data sheet no. 95 for particulars.
- 256 pixels wide
- 256 lines
- 5 MHz clock (probably not typical)



18.8 Sync Generator: Register Contents

Register Contents:

Horizontal (Line) Control

R1	9	Horizontal Front Porch	} Time in "clocks"
R2	33	Horizontal Sync Pulse End	
R3	57	Horizontal Blanking	
R4	312	Line Width – must be even	

Vertical (Frame) Control

R5	4	Vertical Front Porch	} Lines
R6	7	Vertical Sync Pulse End	
R7	21	Vertical Blanking	
R8	276	Frame: 256 lines + 20 lines blanking	

Register 0: Contents 0110 0001 1000

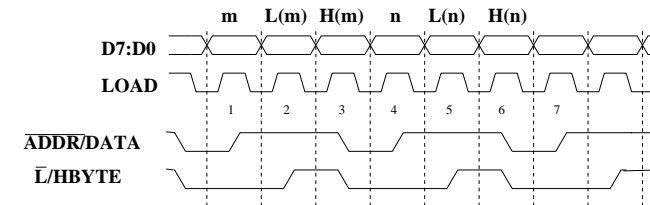
Bit 10: Enable System Clock	1
Bit 9: Disable Equalization	1
Bits 8:5 Sync Pulses Active Low	0000
Bits 4:3 Non-Interlaced	11
Bits 2:0 Default Output Config:	000

Pin 12 CBLANK. Pin 13 HGATE. Pin14 CSYNC. Pin 15 VGATE

18.9 Sync Generator - Manual Mode

□ LM1882 must be loaded on power up.

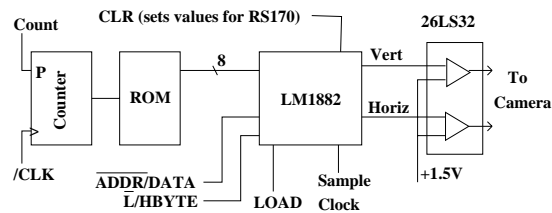
Cycle No.	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load address m
2	Enable Lbyte Data Mode	Load Lbyte m
3	Enable Hbyte Data Mode	Load Hbyte m
4	Enable Manual Addressing	Load address n
5	Enable Lbyte Data Mode	Load Lbyte n
6	Enable Hbyte Data Mode	Load Hbyte n



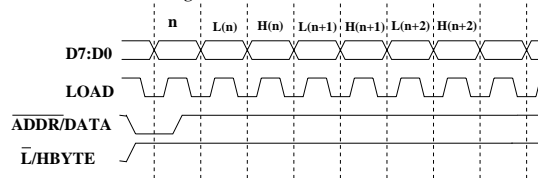
18.10 Sync Generator - Automatic Mode

□ LM1882 must be loaded on power up.

- Use a ROM (PROM) to hold configuration.
- Your MCU or FSM must do the programming.



"Automatic Addressing Mode"



18.11 Sync Separator

□ Operates in reverse direction.

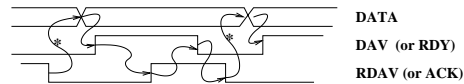
- Generates composite sync from video.
- Generates separated sync signals too.



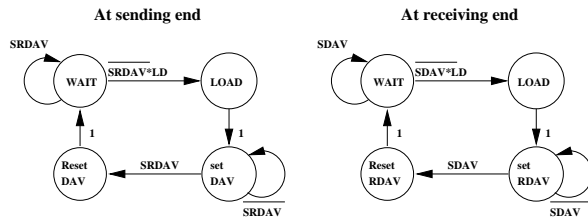
18.12 Getting Information Here to There

□ Full Handshake: Timing

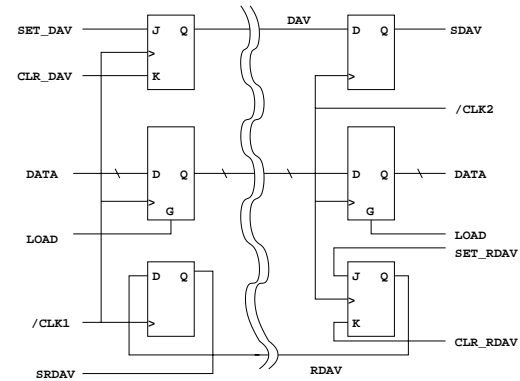
- No data gets lost.
- Simple circuit to do this is on next page.



* and we want to send more data, i.e., LD is true.



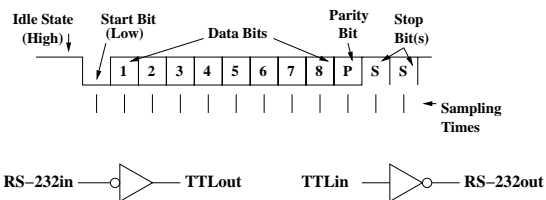
18.13 Parallel Interface, Full Handshake



18.14 Serial Interface

□ RS-232 is a serial interface standard.

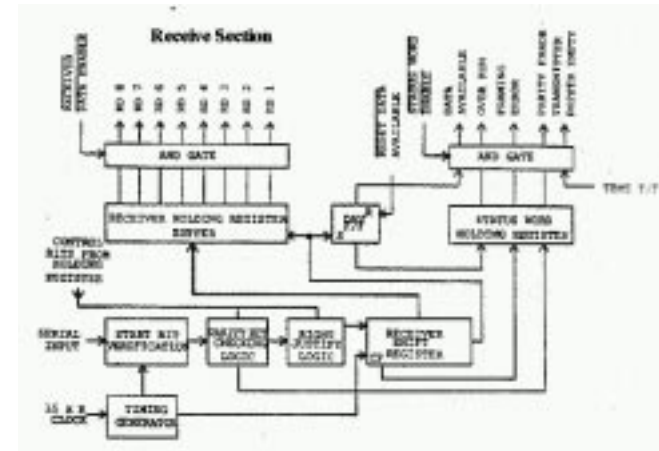
- What is shown here is TTL signal.
- RS-232 levels are inverted from this.
- RS-232 levels are -3 to -15 and +3 to +15 volts.
- MAX 202 has 2 RS-232 to TTL and 2 TTL to RS-232 converters.



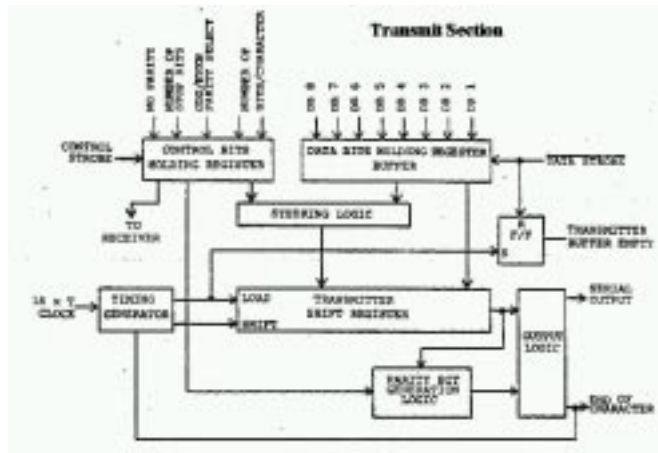
□ UART

- Universal Asynchronous Receiver/Transmitter
- Increasingly less common devices
- Example is the AY-3-1015D (now obsolete but useful).

18.15 AY-3-1015D Receive Section

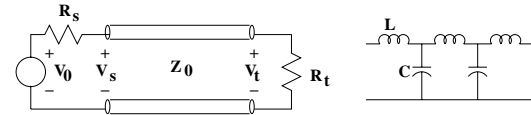


18.16 AY-3-1015D Transmit Section



18.17 Transmission Lines

- Signals travel on wires.
 - Attenuation -- losses
 - Reflections -- affected by terminations



Transmission Line has characteristic parameters:

L : Inductance per unit length
 C : Capacitance per unit length

$$Z_0 = \sqrt{\frac{L}{C}}$$

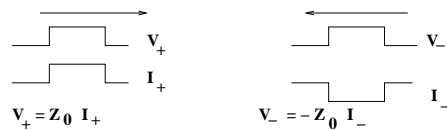
Z_0 : Characteristic Impedance

U_0 : Phase Velocity

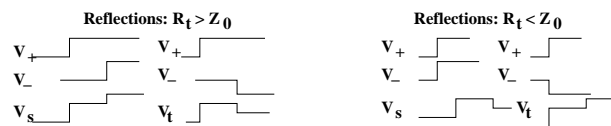
$$U_0 = \sqrt{\frac{1}{LC}}$$

18.18 Signal Propagation

- Pulses traveling on the line
 - Voltage and Current
 - Ratio of voltage to current is 'characteristic impedance'.
 - Sign of that ratio is direction of propagation.
 - Propagate at $< C$ (speed of light).

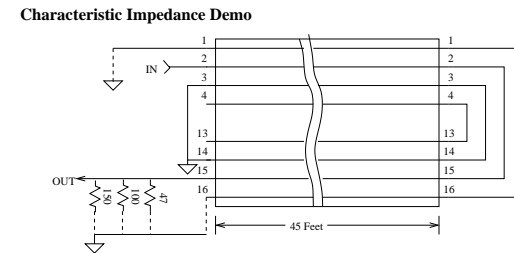


- Pulses are absorbed if receiving end is matched.
- If not matched, pulse 'reflects'.
 - Sign of reflected wave depends on impedance.



18.19 Characteristic Impedance Demo

- Reflections depend on terminating impedance.
 - Can be minimized by terminating correctly.



Lesson here: Terminate Wires in Characteristic Impedance

18.20 Crosstalk Demo

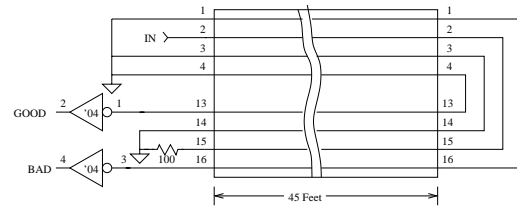
□ Flat Ribbon Cable

- Similar to kit interconnect cables
- Wires situated next to each other
- Capacitive and inductive coupling

□ Crosstalk minimized by grounding alternating wires.

- Ground - Signal - Ground - Signal ...

Crosstalk Demo



Lesson here: Alternate Ground and Signal Wires in Cables