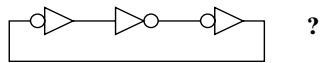
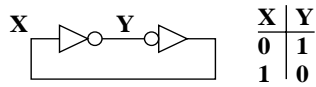


## 4.1 Feedback

Wednesday, February 14, 2001

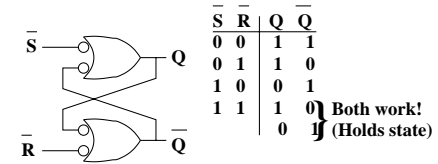
Feedback produces 'State'



What does this one do? →

## 4.2 Latch

S-R Latch (74LS279)

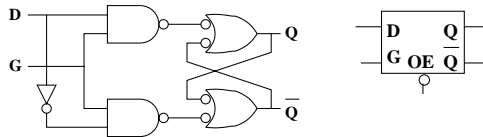


Question: What happens if  $\bar{S}$  and  $\bar{R}$  go 0 to 1 at the same time?

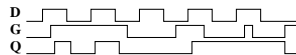
## 4.3 D Latch

D Latch

(74LS373 is an octal latch with tristate.)

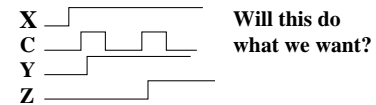
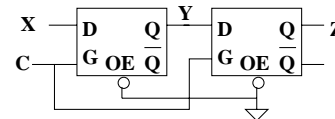


The latch is a "follow and hold":



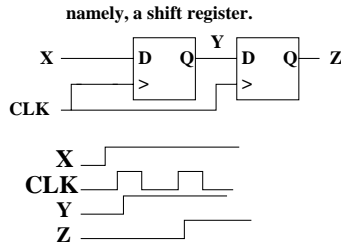
## 4.4 Not a Shift Register

Problem with latches in multi-stage logic



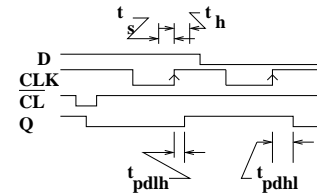
## 4.5 Shift Register

Edge Triggered Flip-Flops can do what we want, namely, a shift register.



74LS74 has two of these. Preset and Clear are active low and asynchronous.

## 4.6 Timing Parameters

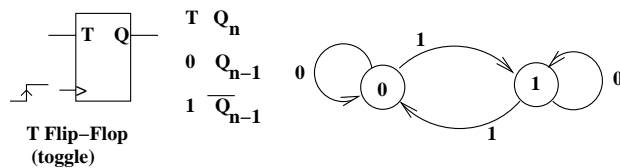
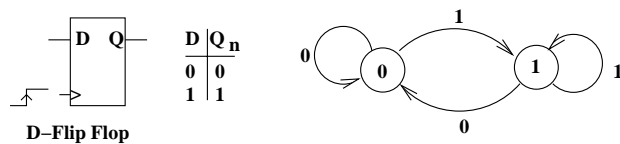


Typical Timing Parameters for 74LS Parts

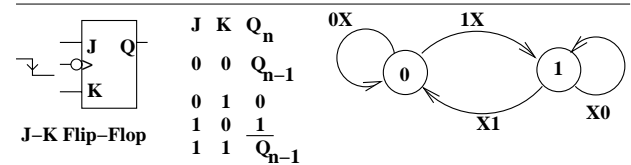
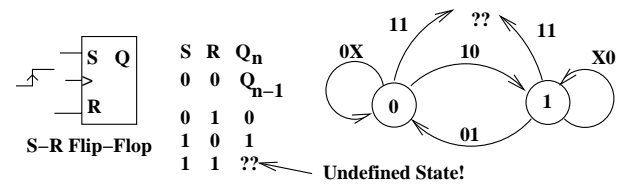
Setup  $t \geq 20$  nS  
 Hold  $t \geq 5$  nS  
 Clock to Q  $\leq 20$  nS  
 CL or PR to Q  $\leq 25$  nS  
 CLK high  $\geq 25$  nS  
 Max Frequency 25 MHz

## 4.7 D and T Flip-Flops

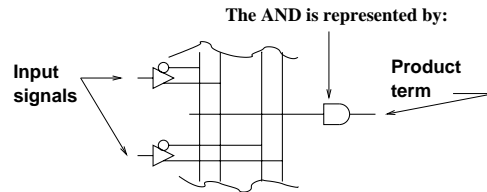
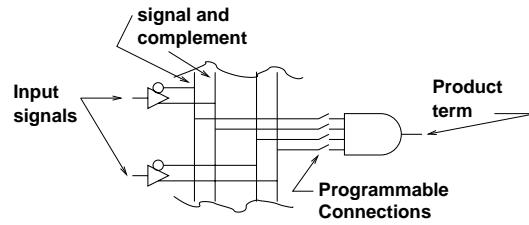
Flip-Flops are Two-State Devices:



## 4.8 SR and JK Flip-Flops

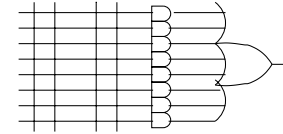


## 4.9 Programmable Logic



## 4.10 Or of Ands

The product terms produced by the ANDs are combined in large ORs.

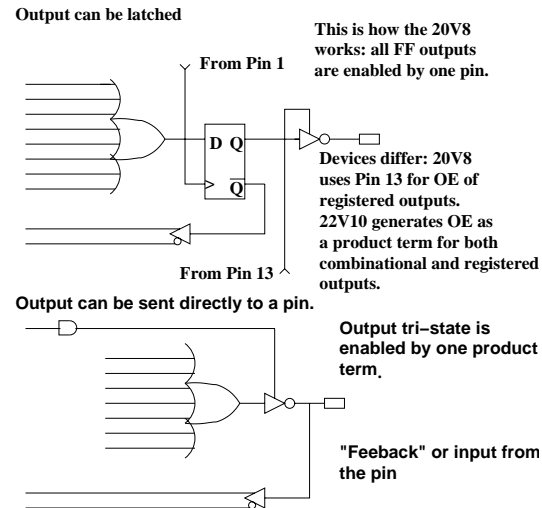


And the output from the OR can be treated in a number of ways .

Pin	20V8(1)		20V8(2)		22V10	
	Use	Terms	Use	Terms*	Use	Terms
23	I		I		I/O	8
22	O	7	I/O	8	I/O	10
21	I/O	7	I/O	8	I/O	12
20	I/O	7	I/O	8	I/O	14
19	I/O	7	I/O	8	I/O	16
18	I/O	7	I/O	8	I/O	16
17	I/O	7	I/O	8	I/O	14
16	I/O	7	I/O	8	I/O	12
15	O	7	I/O	8	I/O	10
14	I		I		I/O	8
13	I		/OE		I	

20V8 (1): All outputs are combinatorial (none registered).  
 (2): Some outputs registered; 8 product terms for registered outputs only.

## 4.11 Outputs



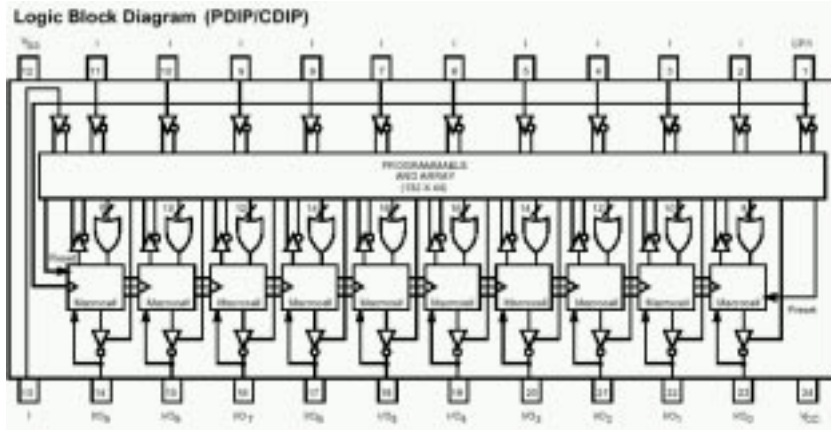
## 4.12 Levels

PALs are CMOS, voltage levels are compatible with TTL.

	20V8	22V10	TTL(74LS00)
$V_{OL}$	0.5 V	0.4 V	0.4 V
$V_{IL}$	0.8 V	0.8 V	0.8 V
$V_{OH}$	2.4 V	2.4 V	2.7 V
$V_{IH}$	2.0 V	2.0 V	2.0 V
$I_{OL}$	24 mA	16 mA	8 mA
$I_{OH}$	-3.2 mA	-3.2 mA	-4 mA
$I_{IL}$	~10 $\mu$ A	~10 $\mu$ A	-4 mA
$I_{IH}$	~10 $\mu$ A	~10 $\mu$ A	20 $\mu$ A

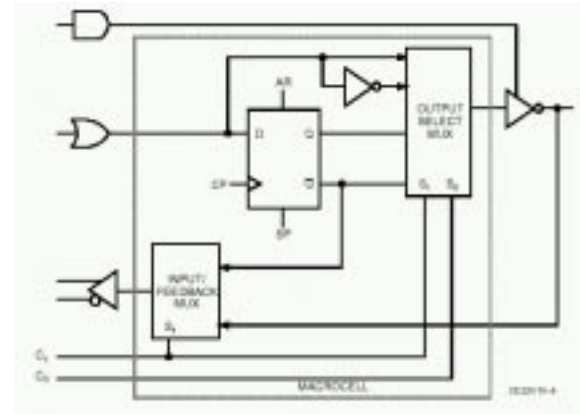
### 4.13 22v10 PAL

- Flexible 'Macrocells'
- 10 Macrocells, varying number of product terms

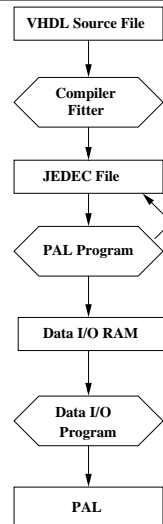


### 4.14 22v10 Macrocell

- **Enable is a product term.**
- Output is registered or direct.
- Feedback is registered or from a pin.



### 4.15 Programming Small PALs



### 4.16 CY7C374i

Manufacturer is Cypress (URL is <http://www.cypress.com>). Information about the 370 family and the data sheet for the CY7C374i are on the web page.

128 macrocells in eight blocks

64 I/O pins

5 dedicated inputs including 4 clocks

which are not usable on the 6.111 CPLD board.

JTAG interface - ISR - In-System Reprogrammable

High Speed

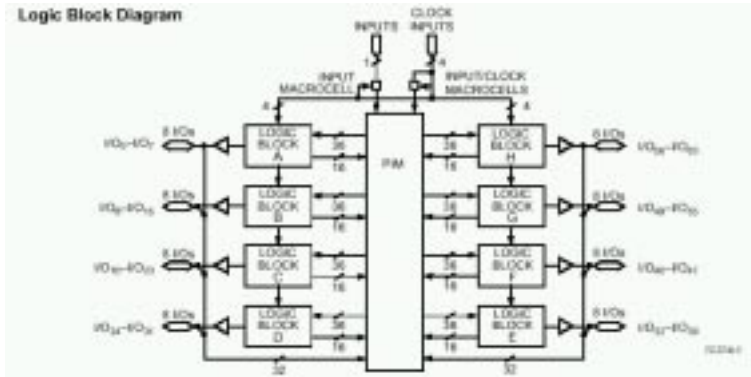
$f_{max} = 125 \text{ Mhz}$

$t_{PD} = 10 \text{ ns}$

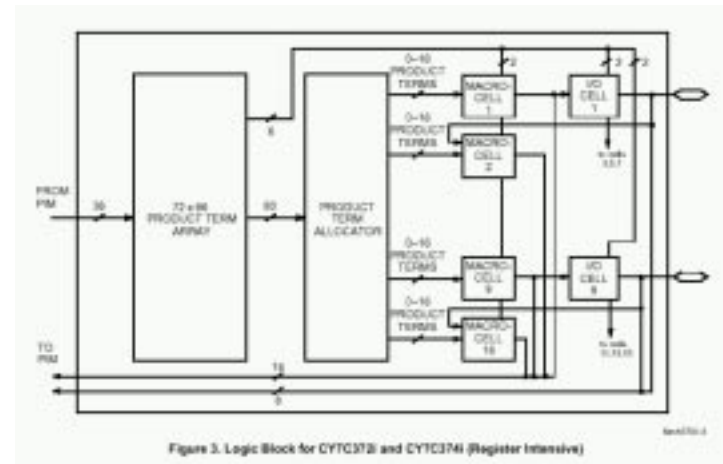
$t_S = 5.5 \text{ ns}$

$t_{CO} = 6.5 \text{ ns}$

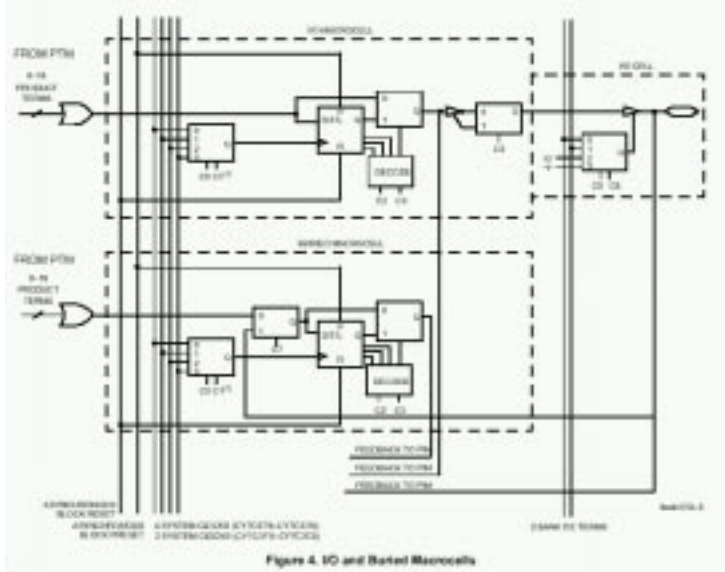
### 4.17 CY7C374i Block Diagram



### 4.18 CY7C374i Logic Block (1 of 8)



### 4.19 CY7C374i Macrocells



### 4.20 I/O in more detail

