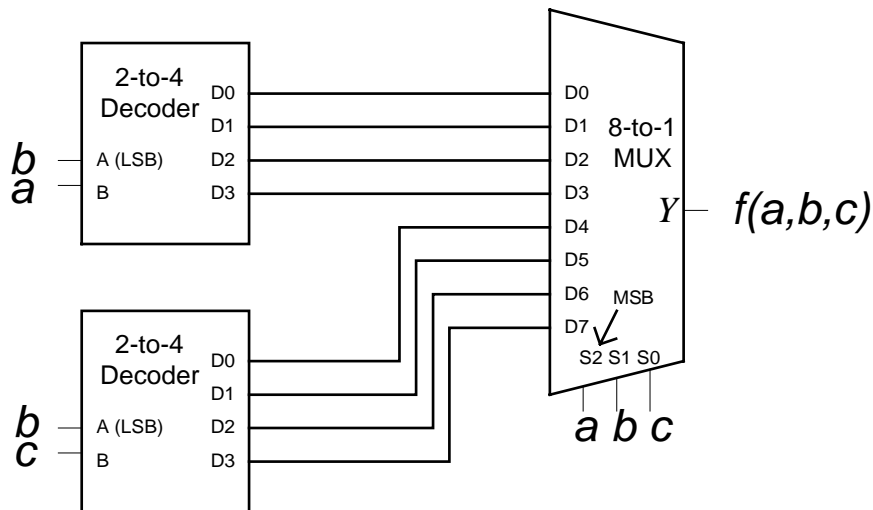


Massachusetts Institute of Technology
 Department of Electrical Engineering and Computer Science
 6.111 – Introductory Digital Systems Laboratory
 Problem Set # 2

Issued : Wednesday February 14, 2001
 Due : Wednesday February 21, 2001 (IN CLASS)

Problem 1: Fun with Combinational Logic !!!

1. Find the MSP and MPS form of the function realized by the circuit shown below.



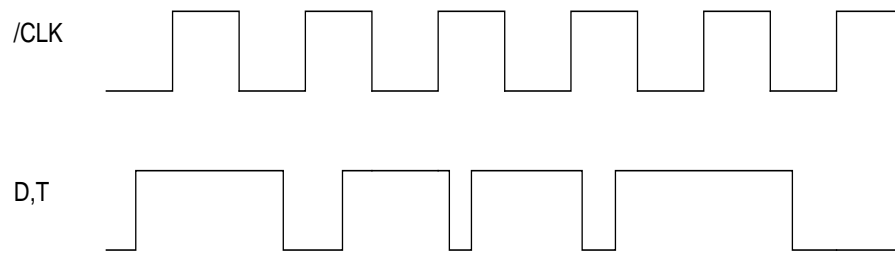
2. Can you implement the above logic with a 3-to-8 decoder and NAND gates.

Problem 2: More Combinational Logic !!!

1. Design the logic that multiplies two 2-bit numbers $(x_1x_0)_2$ and $(y_1y_0)_2$ using only NAND gates. The product should be a 4-bit number $(p_3p_2p_1p_0)_2$.

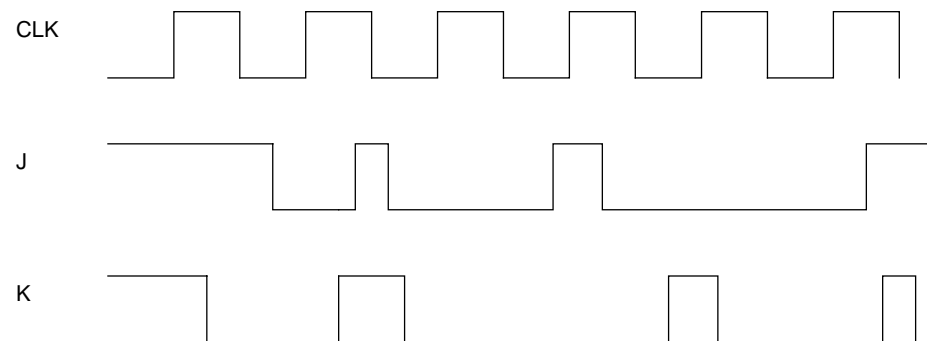
Problem 3: Thou shall know his Flip-Flops !!!

Using the following timing diagram, draw the output Q (assuming Q starts at 0) for a positive-edge triggered D flip-flop, positive-edge triggered T flip flop, and positive-edge triggered JK flip-flop.



Q(T)

Q(D)



Q(JK)

Problem 4: Counter Theory !!!

1. The '163 is a synchronous counter while a '393 is a ripple counter. What does this mean? Comment on their differences (design, performance, area, etc.)
2. Implement a '163 counter in VHDL. You may want to refer to the TTL Data book for complete functionality.
3. There are multiple ways to create an 8-bit counter from two '163's. One technique involves wiring the RCO of the first counter to be the clock input of the next counter. While this circuit would give you the right results, it is a bad way of cascading counters. Can you explain why? How would you cascade counters? Do it in VHDL using a *hierarchical* approach to yield an 8-bit equivalent of the '163.

REVISED on 2/16/01

Problem 5: Shifters !!!

A)) Implement in VHDL one basic cell (1 bit) of a n-bit shift register. The basic cell has 2 control inputs S0 and S1 and 3 data inputs SR, SL, and DI. SR is input data being shifted in from the right, SL is input data being shifted in from the left, and DI in parallel load data.

The function of your cell is

S1	S0	Function
0	0	Shift Right
0	1	Shift Left
1	0	Synchronous data hold
1	1	Synchronous parallel load

B) Use that implementation, i.e. hierarchy, to make a 4-bit shifter in VHDL. The function of the 4 bit shifter is

S2	S1	S0	Function
0	0	0	Shift Right (all 4 bits)
0	0	1	Shift Left (all 4 bits)
0	1	0	Synchronous data hold
0	1	1	Synchronous parallel load
1	0	0	Synchronous preset MSB to 1 and clear other bits
1	0	1	Synchronous common clear (all 4 bits)

C) Simulate the 4-bit shifter you created in Part C) and show your results (*optional*).