**Massachusetts Institute of Technology**
**Department of Electrical Engineering and Computer Science**
**6.111 - Digital Systems Labratory**
**Problem Set #3**

Issued : Wednesday February 21, 2001
Due : Wednesday February 28, 2001(**IN CLASS**)

## Problem 3.1 Counters

Using the minimum amount of logic, configure the LS163 4-bit counter to count:

a. from 3 to 12 repeatedly. ie. 3, 4, 5, ..., 11, 12, 3, 4, 5

b. from 0 to 5, skip 6 through 10, then count 11 to 13 before resetting to 0. ie. 0, 1, ..., 5, 11, 12, 13, 0, 1, ...

c. the sequence 0, 1, 2, 4, 7, 11, 13, 14 over and over again.

## Problem 3.2 Finite String Recognizer

A finite string recognizer has one input, X, and one ouput, Z. The output is asserted whenever the input sequence ...010... has been observed, as long as the sequence 100 has never before been seen. Design this Finite State Machine (FSM) with the least number of states possible.
(Hint: < 9 states are required for this state machine)

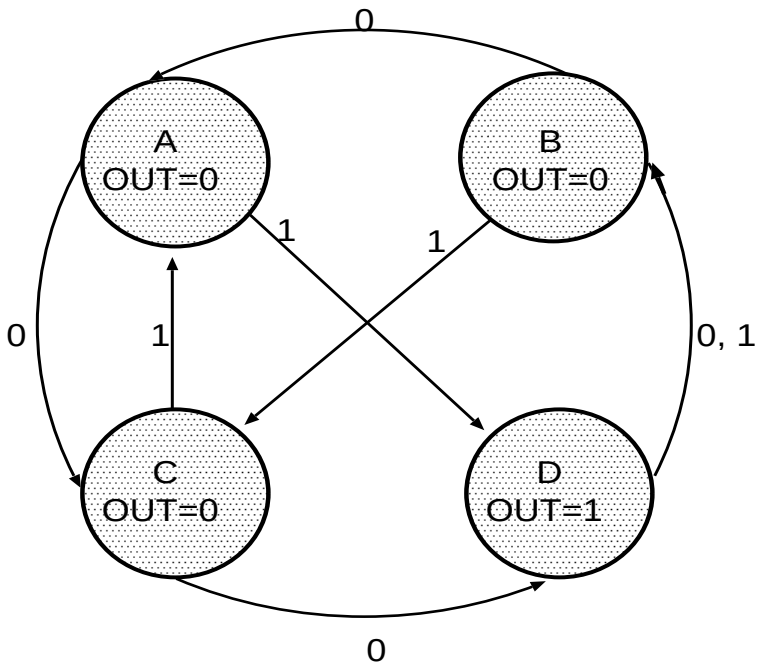
Here are some sample input and ouput strings to clarify the FSM specification:
X: 00101010010...
Z: 00010101000...

X: 11011010010...
Z: 00000001000...

Turn in your state diagram, carefully labeled. Be sure to indicate which state the FSM is in after a reset.

**Problem 3.3 One More State - Transition Diagram**

Consider the following state-transition diagram:

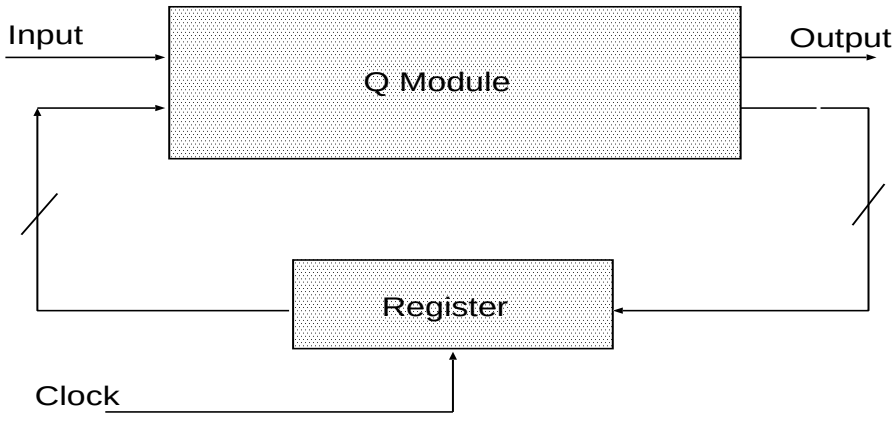



For each of the following questions, assume that the machine starts at state A.

a. Give the sequence of states visited, and the sequence of outputs produced, if a machine described by the above transition diagram is presented with the input string 00110.

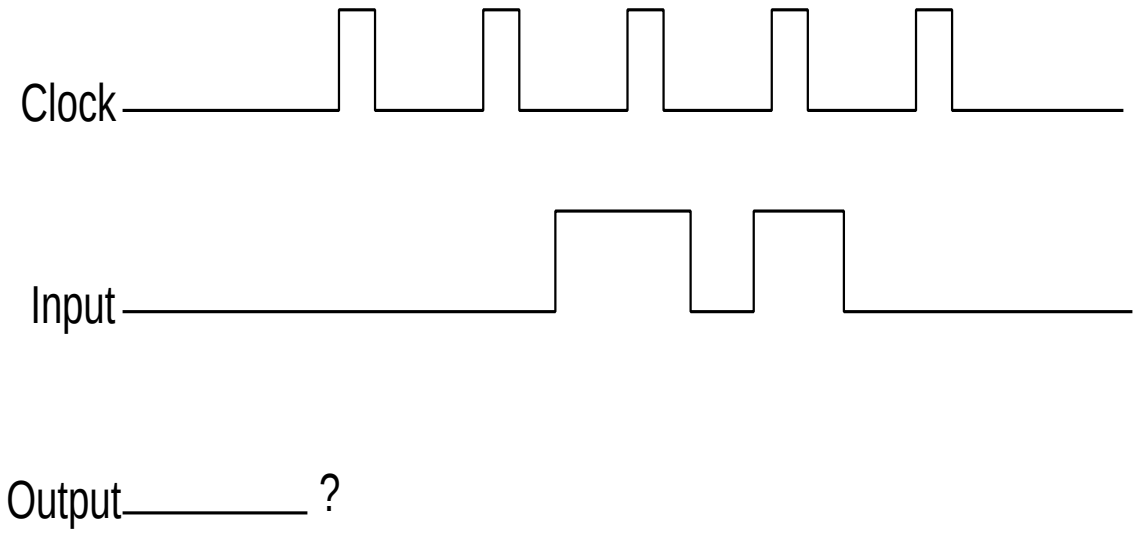
b. What is the only string of inputs that will yield an output string composed entirely of 0s?

c. The state - transition diagram is implemented in a clocked sequential machine, shown below, consisting of a register of positive edge-triggered D flip-flops and a "Q module", which is purely combinational logic. How many state variables are needed?

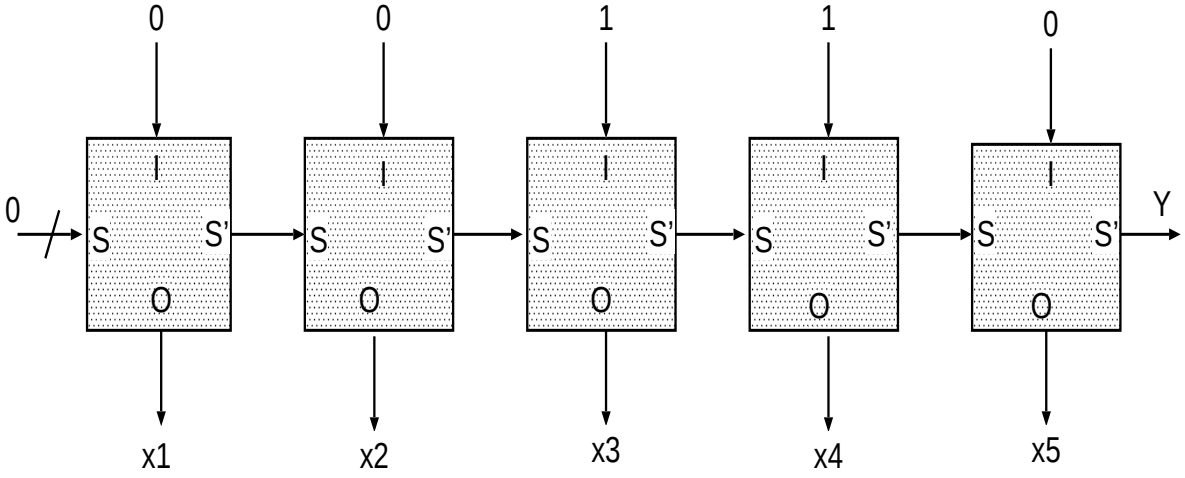


d. Give the truth table for the Q module such that the sequential machine above implements the desired state-transition diagram. Make sure that the initial state (A) corresponds to all state variables being zero.

e. Reproduce the diagram below and fill in the line for the output for the sequential machine using the Q module and D flip-flops. You may neglect propagation delay in the logic, assuming them to be zero.




F. In the arrangement of Q modules shown below, what outputs will be produces at X1, X2, X3, X4, X5, and Y?




G. Implement the FSM described above (with a single Q module) in VHDL. Turn in your code.