

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 — Introductory Digital Systems Laboratory

FPGA Module
Revised (May 29, 2002)

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1 WARNING - BURN OUT

A number of students have burned out FPGAs. The following describes the probable cause. This has not been confirmed by experiment. I really don't want to perform this experiment. The FPGAs that have been fried are the 10K70 (the right hand one). The 10K70 is surface mounted and it is expensive to replace. In addition, the pc board is often damaged in trying to replace it. We have a limited number of pc boards!

Altera states that unused pins **MUST** be unconnected. This is not possible for the pins connected to the AD bus (see below). All of these pins must be used as inputs, outputs, or specifically tri-stated. In addition, all pins that are connected to a 50 pin connector (see below) should be used as inputs, outputs, or specifically tri-stated.

Unfortunately, there is no easy way to tristate unused pins. Altera literature says that unused pins are grounded and **MUST** be unconnected. Unused pins must be specifically listed in the top level entity and specifically tri-stated.

Please use the 10K10 (on the left) until you are familiar with the use and programming procedures. This device is in a socket and at least we can replace it if you burn it out.

2 FPGA Module

The FPGA module consists of two of Altera's FLEX 10K PLDs, one FLEX 10K10 and one FLEX 10K70, which can be accessed through the lab kit's NuBus interface and 50-pin ribbon cable connectors. The state of the NuBus interconnects can be continuously displayed on the lab kit's hex leds by connecting jumpers /LHEX and /HHEX to /CLK (or any other clock). Also, the Proto strip connection labeled NUHEX must be grounded.

¹This document has been modified from the original version written by Brian Perrin April, 4, 2002.

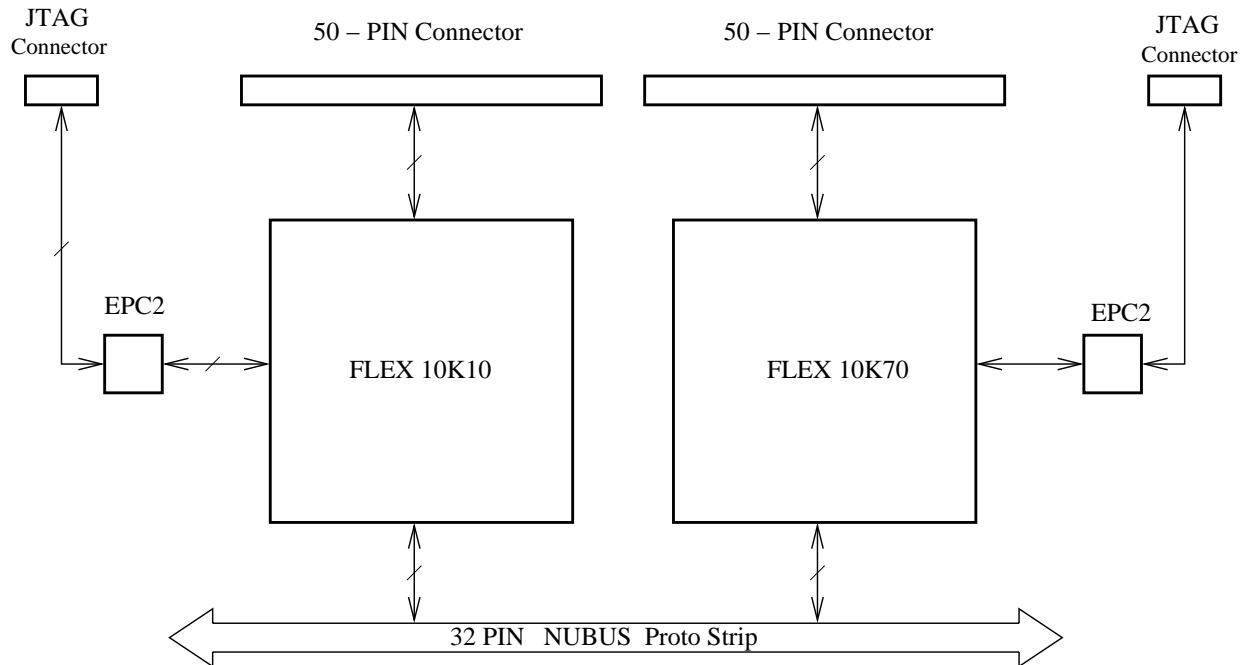


Figure 1: FPGA Module Block Diagram

The 50-pin ribbon cable connectors can be fed directly into the inputs of the Logic Analyzer via 50-pin connectors on the kit. Note that each gate array has its own 50-pin connector which can be connected either to the K1 or K2 connectors on the kit. BEWARE, the signals which are grounded by the K1 and K2 connectors are different! It is never a good idea to use EDGEd signals on the 50-pin connectors. Use only “levels” and wait for the ringing to settle down before sampling them.

Most of the NuBus connections are to I/O pins, but two clock pins are on the NuBus proto strip. Each gate array has two clocks. Which one(s) are used is specified by your VHDL code. In addition one of the clocks is connected to an I/O pin on each gate array. Note that A31 is used for supplying the clock to the CPLD module if one is also used.

Information on the Flex devices can be found on Altera’s web site. The URL is <http://altera.com/products/devices/flex10k/f10-index.html>. From there, you can click on Data Sheets and find <http://altera.com/literature/lit0f10.html> and then click on the first data sheet. This tells you more than you want to know! Please don’t print it out unless you really want to save the paper copy – it is 128 pages long! Pages 5 through 15 give you a good summary of capabilities.

This data sheet tells you that the 10K10 has 10,000 gates and 576 logic elements while the 10K70 has 70,000 gates and 3744 logic elements. That is a lot of capability. Even badly written VHDL code is likely to fit!

3 Programming Overview

The gate arrays are SRAM based which means they need to be configured each time power is applied. Happily, this is done automatically as the gate arrays are wired to a flash prom (EPC2). However, one does have to program the EPC2. This is done by the Max+plus II software using information in a `<project_name>.pof` file and communicating with the EPC2 via a JTAG interface.

You must generate the appropriate `<project_name>.pof` file by selecting the appropriate device (EPF10K10LC84-3 or EPF10K70RC240-2 and the configuration device option of EPC2LC20). See the beginner's guide for details on how to do this.

There is no simple (quick) way to erase the EPC2s. Instead one must “erase” them by programming them with a VHDL file which tri-states all of the I/O pins connected to either the NuBus interface or the 50-pin connector (should you ever use it). This should be done whenever you use a new (to you) FPGA Module. Then all you need do is to program your FPGAs. Of course you want to make sure that the two FPGAs never drive the same pin on the NuBus interface, e.g., AD13.

4 Programming

The following steps are the programming procedure:

Set up your lab kit next to a computer with a programmer (BitBlaster) attached to it. Currently the Sun Ultra 5s in the lab have a BitBlaster installed. Turn on the lab kit.

Insert the 10-pin ribbon connector from the programmer into the 10-pin connector socket corresponding to the FLEX 10K PLD you wish to program; the left connector programs the FLEX 10K10, the right connector programs the FLEX 10K70. Be sure the orientation of the cable in the socket is correct by lining up the notch on the socket with the groove on the cable. The green light on the programming box connected to the cable should light up. If the green light is not on, then likely the kit power is not on or the cable is in backwards.

Using Altera's MaxPlus2 software, load the **Programmer** module (from the **MAX+plus II** menu). If this is the first time you are using the programmer, a hardware configuration window will appear. The following assumes the computer you are using is an Ultra 5. The RS-232 box should read `/dev/term/a` and the baud rate should be 38,400 which should match the switch settings on the BitBlaster programming box. You can edit the hardware configuration any time by clicking on **Options>Hardware Setup**.

To speed up the programming process turn off the automatic blank check and verify. Click on **Options>Programming Options** to get a pop-up window. If any of these options are selected, then de-select them.

Be sure **Multi-Device JTAG Chain** is selected in the **JTAG** menu, then select **Multi-Device JTAG Chain Setup...** from the **JTAG** menu. In the new window, select **EPC2** as the **Device Name**, and select the programming file using the button. You want the **.pof** version of your compiled code. After choosing the file, click the **Add** button and then **OK**.

Click the **Program** button to program the file. x Programming will take a while. When the programmer is done, it will return a “Programming Successful” message. Your new program will not take effect until you turn the lab kit off and back on again.

5 NuBus Interface

There are thirty I/O pins from each FLEX 10K PLD connected to the NuBus interface, as well as to each other.

Two clock pins are on the NuBus proto strip. Each gate array has two clocks. Which one(s) are used is specified by your VHDL code. In addition one of the clocks is connected to an I/O pin on each gate array so that the I/O pin can be used if only one clock is used. Note that A31 is used for supplying the clock to the CPLD module if one is also used. The clock pins are denoted in Table 1 as **CLK**.

Table 1: Correlation between NuBus Pins and FLEX 10K Pins

| NuBus Address | FLEX 10K10 Pin Number | FLEX 10K70 Pin Number |
|--------------------------|----------------------------------|----------------------------------|
| A0 | 1 (CLK) | 91 (CLK) |
| A1 | 43 (CLK) | 212 (CLK) |
| A2 | 17 | 7 |
| A3 | 18 | 8 |
| A4 | 19 | 9 |
| A5 | 21 | 12 |
| A6 | 22 | 13 |
| A7 | 23 | 14 |
| A8 | 24 | 15 |
| A9 | 25 | 17 |
| A10 | 27 | 18 |
| A11 | 28 | 19 |
| A12 | 29 | 20 |
| A13 | 30 | 21 |
| A14 | 35 | 24 |
| A15 | 36 | 25 |
| A16 | 37 | 28 |
| A17 | 38 | 29 |
| A18 | 39 | 30 |
| A19 | 47 | 31 |
| A20 | 48 | 33 |
| A21 | 49 | 34 |
| A22 | 50 | 35 |
| A23 | 51 | 36 |
| A24 | 52 | 38 |
| A25 | 53 | 39 |
| A26 | 54 | 40 |
| A27 | 58 | 41 |
| A28 | 59 | 43 |
| A29 | 60 | 44 |
| A30 | 61 | 45 |
| A31 | 62 | 46 |

6 50-pin Ribbon Cable Interface

There are two 50-pin ribbon cable connectors on the FPGA module. The one on the left accesses only pins from the FLEX 10K10 PLD, while the one on the right accesses only pins from the FLEX 10K70 PLD. The FLEX 10K10 50-pin connector provides access to an additional 21 pins, while the FLEX 10K70 50-pin connector provides access to an additional 25 pins. Some of the pins on the FLEX 10K10 are input only, designated by **IN** on Table 2.

The signals on the 50-pin connectors are fed directly into the three L interfaces for use with the Logic Analyzer, depending on which connector is used to connect with the FPGA module. Be certain that signals labelled as **GND** are either grounded or left floating in the FLEX 10K PLD programming, as these signals are set by the lab kit.

Table 2: Correlation between Ribbon Cable Pins and FLEX 10K Pins

| FLEX 10K10 Pin Number | FLEX 10K70 Pin Number | K1 Connector Interface | K2 Connector Interface |
|----------------------------------|----------------------------------|-----------------------------------|-----------------------------------|
| - | 80 | L1-0 | L2-8 |
| - | 79 | L1-1 | L2-9 |
| - | 78 | L1-2 | L2-10 |
| - | 76 | L1-3 | L2-11 |
| 81 | 75 | L1-4 | L2-12 |
| 80 | 74 | L1-5 | L2-13 |
| 79 | 73 | L1-6 | L2-14 |
| 78 | 72 | L1-7 | L2-15 |
| 72 | 71 | L1-8 | GND |
| 71 | 70 | L1-9 | L3-0 |
| 70 | 68 | L1-10 | L3-1 |
| 67 | 67 | L1-11 | L3-2 |
| 66 | 66 | L1-12 | L3-3 |
| 65 | 65 | L1-13 | L3-4 |
| 11 | 64 | L1-14 | L3-5 |
| 10 | 63 | L1-15 | L3-6 |
| 9 | 62 | GND | L3-7 |
| 8 | 61 | L2-0 | L3-8 |
| 7 | 56 | L2-1 | L3-9 |
| 6 | 55 | L2-2 | L3-10 |
| 5 | 54 | L2-3 | L3-11 |
| 84 (IN) | 53 | L2-4 | L3-12 |
| 44 (IN) | 51 | L2-5 | L3-13 |
| 42 (IN) | 50 | L2-6 | L3-14 |
| 2 (IN) | 49 | L2-7 | L3-15 |