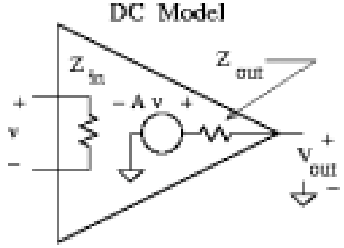
L15.1 Operational Amplifiers

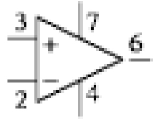
DC Model



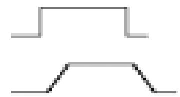
	Ideal	'741	'357
A	∞	$\frac{200{,}000}{f\,(Hz)}$	$\frac{20 \times 10^6}{f\,(Hz)}$
Z_{out}	0	75 Ohms	
Z_{in}	∞	300 kOhms	10^{12} Ohms

Don't forget to wire the Power Supply!

8−Pin "Mini−Dip"



Slew Rate:



'741: 0.5 V/μ sec
'357: 50 V/μ sec

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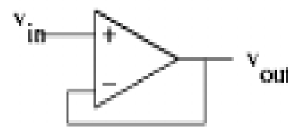
L15.2 Uses of Op Amps

Negative feedback drives the + input to (nearly) the same potential as the − input.

Follower

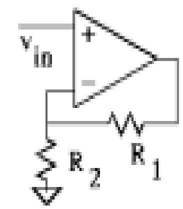


$v = v_{in} - v_{out}$

$v_{out} = A\,(v_{in} - v_{out})$

$v_{out} = \frac{A}{1+A}\, v_{in}$

Non−Inverting Amplifier



$v_{in} = v_{out} \frac{R_1}{R_1 + R_2}$

$v_{out} = \frac{R_1 + R_2}{R_1}\, v_{in}$

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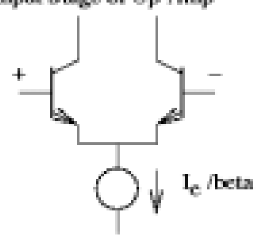
L15.3 Inverting and Differential Amplifiers

Resistance seen by the plus and minus inputs should be the same when an op amp is configured for voltage gain.

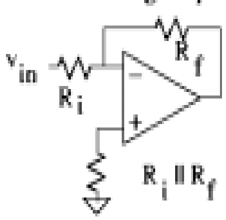
Bias currents (relatively equal) times difference in input resistance look the same as an input signal.

Bipolar input stage draws some bias current.
FET input stage draws very little input current.

Input Stage of Op Amp



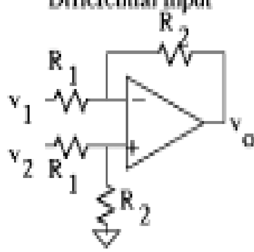
Inverting Amp



$\frac{v_{out}}{R_f} = -\frac{v_{in}}{R_i}$

$v_{out} = -v_{in} \frac{R_f}{R_i}$

Differential Input



$v_{out} = \frac{R_2}{R_1}(v_1 - v_2)$

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L15.4 Comparator / Positive Feedback

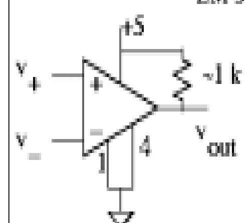
Analog Comparator

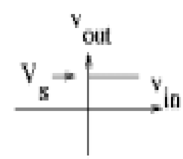
Is V+ > V− ?
The Output is a DIGITAL signal.

The external pull−up resistor is often forgotten.

Analog Comparator: Analog to TTL

LM 311 Needs Pull−Up

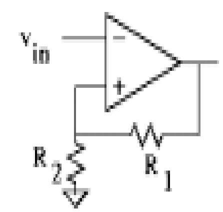


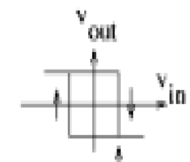


A Schmitt Trigger squares up signals.

Op Amp as Schmitt Trigger:

Output has hysteresis

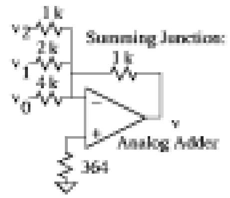




$\frac{R_2}{R_1 + R_2} V_s$

L15.5 D to A Converters

Simple D to A

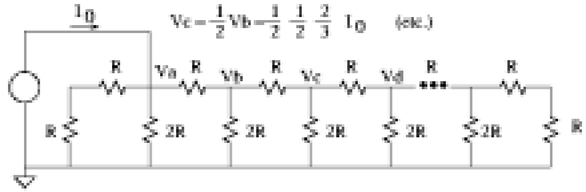


If V+ is at zero potential
then so is V−.
The output voltage is
proportional to sum of currents.
Currents are inversely
proportional to the resistances
IF the input voltages are the same.

Digital To Analog Converters: Use R − 2R Ladder.
Driving Point Impedance is 2/3 R.
Voltage Divider Ratio, Node−Node, is 1/2.

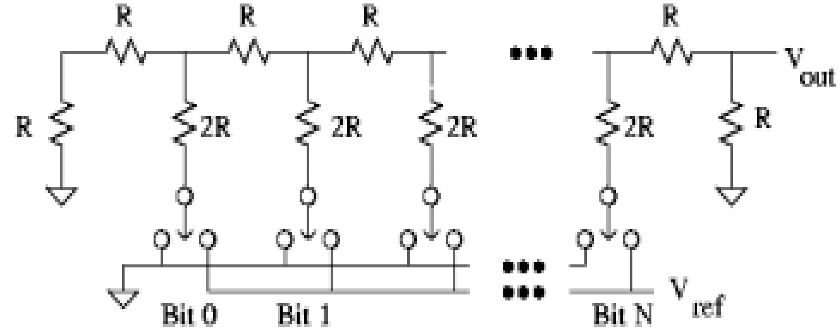
$Va = \frac{2}{3}\ I_0$ $\quad Vb = \frac{1}{2}\ Va = \frac{1}{2}\ \frac{2}{3}\ I_0$

$Vc = \frac{1}{2}\ Vb = \frac{1}{2}\ \frac{1}{2}\ \frac{2}{3}\ I_0$ (etc.)



L15.6 How to build a D to A

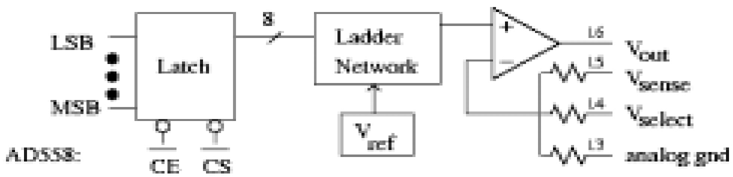
Real D to A converters use a voltage reference and transistor (bipolar or MOS) switches.
Note that the driving point impedance (resistance) is the same for each cell.



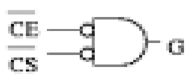
$$V_{out} = \frac{1}{6} V_{ref}\ [\,B_7 + \frac{1}{2} B_6 + \frac{1}{4} B_5 + \ \dots\ + \frac{1}{128} B_0\,]$$

L15.7 AD 558

8−Bit D to A converter that you will use in Lab 3



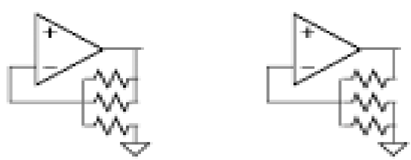
This is a Latch: Data goes through when G = HIGH



Output is very noisy when input bits are settling.
It's best to have inputs stable before latching the input data.

Much like a non−inverting operational amplifier.

Strap Output For Different Voltage:



0 to 2.5 volts

0 to 10 volts
Needs a 12 volt supply!

L15.8 A to D Conversion

Harder than Digital to Analog

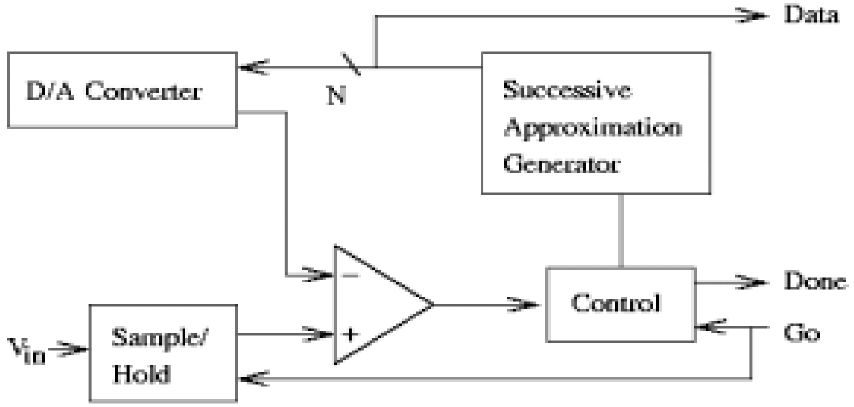
Several Different Methods are Used. We will focus on two methods.

Multiple Conversions (FLASH)
- Very fast
- Used for converting TV signals.
- Difficult to make in high precision.
- AD 775

Successive Approximation
- Medium speed
- Can be economical
- AD 670

L15.9 Successive Approximation A to D

Successive Approximation A/D (e.g. AD 670)

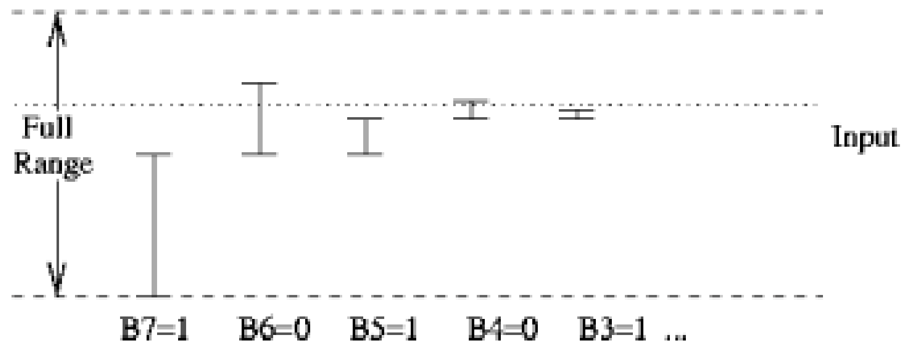


Medium Speed: Conversion Time is bounded by word width.

L15.10 Operation of a Successive Approximation A to D

Set one bit at a time.
D to A generates analog voltage which is compared to the input voltage.
If D to A voltage > input voltage then set that bit; otherwise, reset that bit.
This type of A to D takes a fixed amount of time proportional to the bit length.

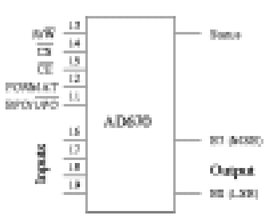
Successive Approximation A/D operation



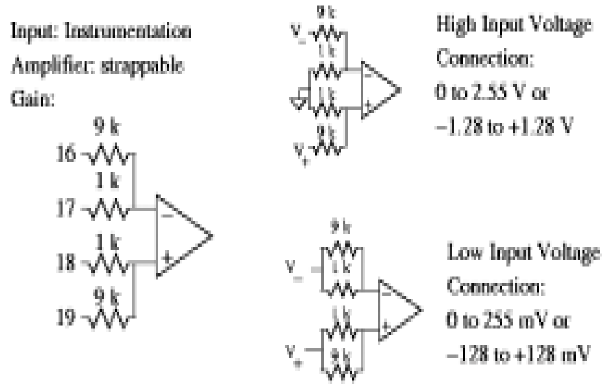
L15.11 AD 670

10 microsecond conversion time

Internal reference voltage
Multiple input ranges
Two output formats

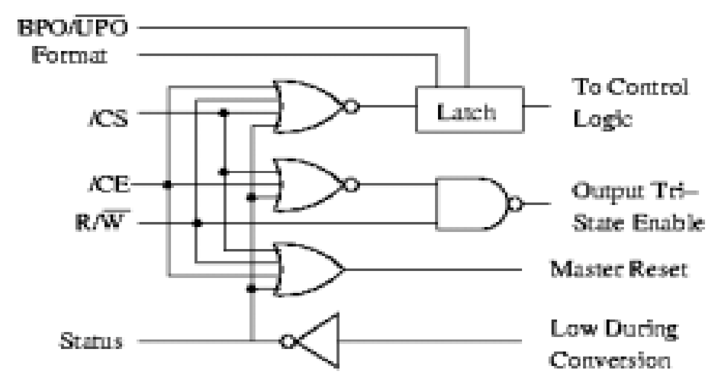


High Input Voltage Range − strap pins 17 and 18 to GND.
Low Input Voltage Range − strap pins 16 to 17 and 18 to 19.



L15.12 Control Logic for AD 670

BPO/UPO	Format	Input Range	Output
0	0	Unipolar	Binary
1	0	Bipolar	Binary
0	1	Unipolar	2's Complement
1	1	Bipolar	2's Complement



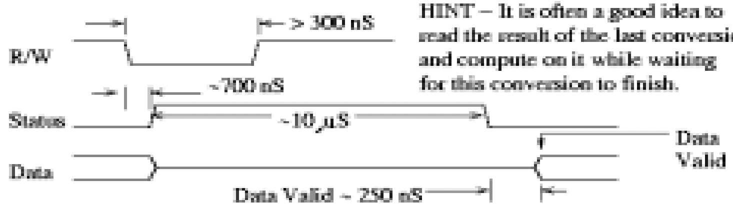
L15.13 Timing for AD 670

Single Conversion Cycle: Short W valid

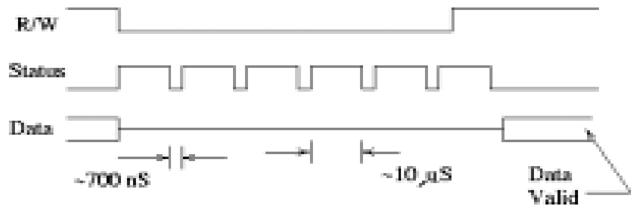
Control bits are /CE, /CS and R/$\overline{W}$
For most uses, tie /CE, /CS to GND

Hold R/W low. Must wait for last to finish.
Need to control these if connected to a bus!

HINT – It is often a good idea to read the result of the last conversion and compute on it while waiting for this conversion to finish.

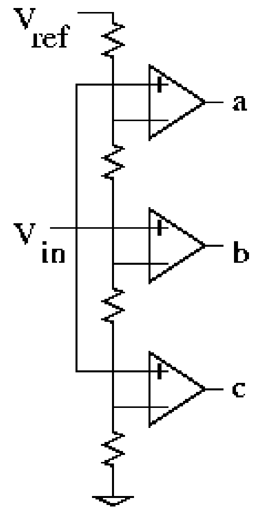


Conversion initiated by R/W LOW pulse



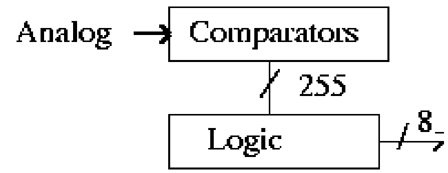
L14514 Flash Converter

"Flash Converter"

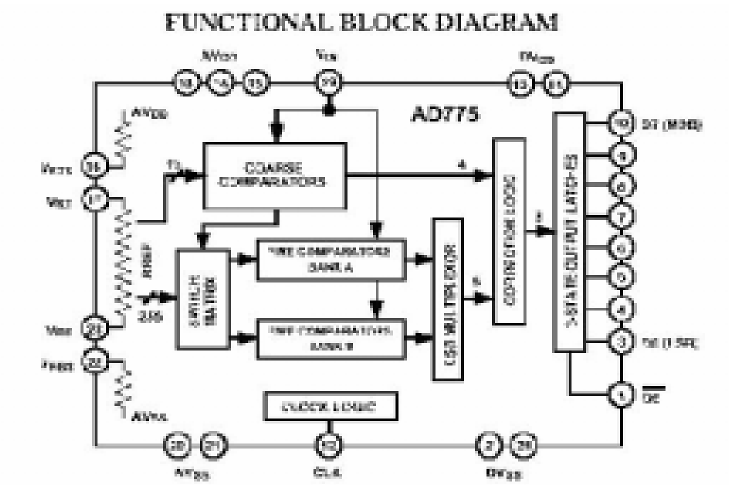


V_{in}/V_{ref}	a	b	c
0–.25	0	0	0
.25–.5	0	0	1
.5 – .75	0	1	1
.75 – 1	1	1	1

2–Bit Converter Needs 3 Comparators.
8–Bit Converter Needs 255 Comparators.
(But is very fast)



L15.15 AD 775 Functional Block Diagram

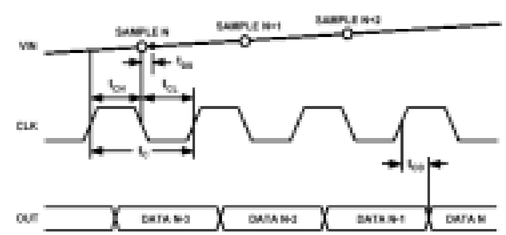


L15.16 AD 775 Timing

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate		20	35		MHz
Clock Period	t_C	50			ns
Clock High	t_{CH}	25			ns
Clock Low	t_{CL}	25			ns
Output Delay	t_{OD}		18	30	ns
Pipeline Delay (Latency)				2.5	Clock Cycles
Sampling Delay	t_{DS}		4		ns
Aperture Jitter			30		ps

Specifications subject to change without notice.

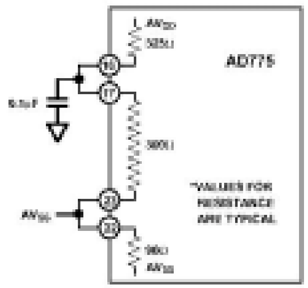


L15.17 Voltage Reference

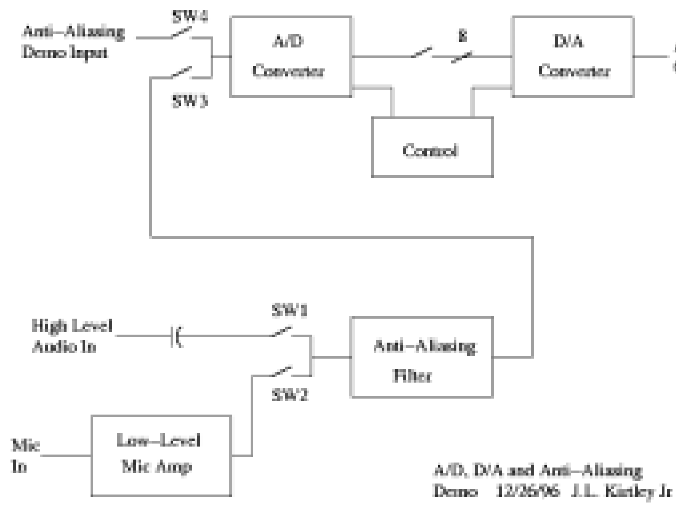
Similar to other flash converters
- Needs a stable reference voltage.
- Different ranges of voltage are defined by the top and bottom of ladder.

Caution is required: the ladder is fragile!
- Voltage range is < 2.8 volts.
- Linearity suffers if < 1.8 volts.
- AVss means "Analog Voltage" (supply).

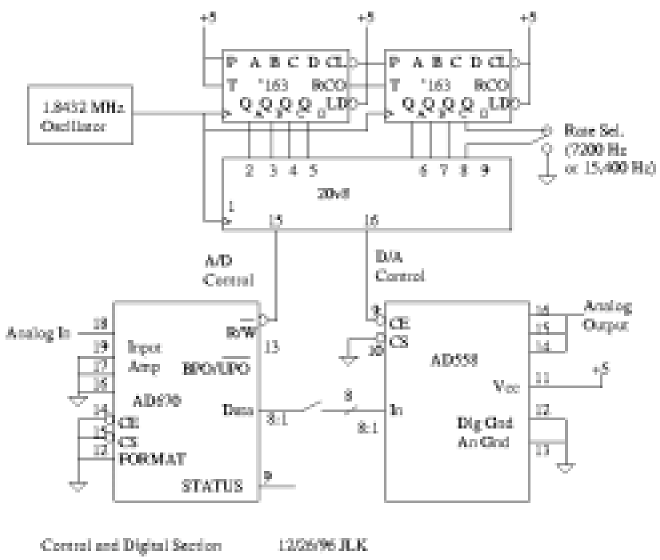
Read the
Data Sheet!



L15.18 A to D , D to A, and Aliasing Demo



L15.19 Control and Digital Section



L15.20 Analog: Gain and Anti−Aliasing