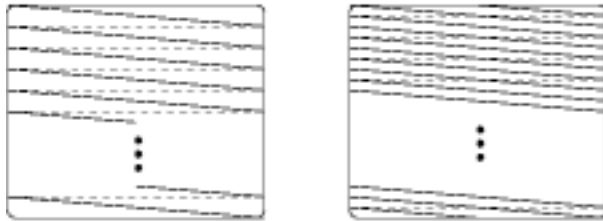


L17.1 Video Displays

Television and most computer displays use raster-scan.
 We will always use non-interlaced formats.

Video (Raster-Scan) Displays are like Television



Non-Interlaced: Frame rate may be 60, 72, etc. frames/sec.

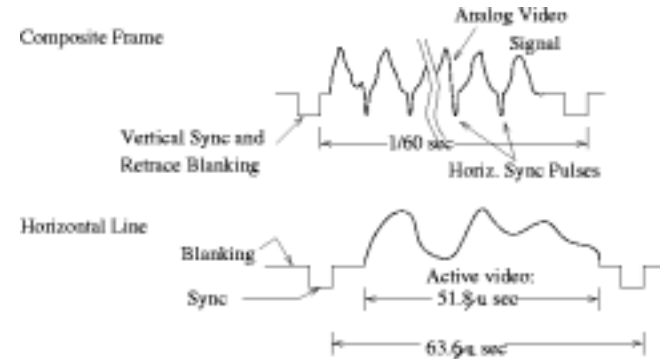
— Scan line
 - - - - - Retrace line

Electron beam "scans" tube. Beam location is shown here. Beam current determines brightness of display.

Interlaced: Frames alternate. This is like television: 60 half frames/sec.

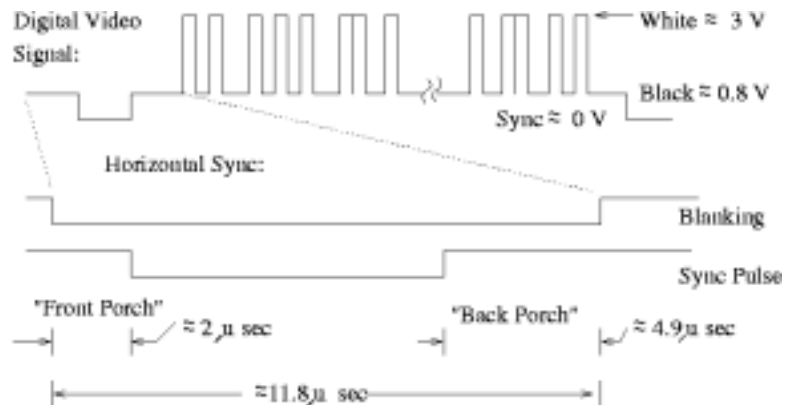
L17.2 Composite Frames

The 'frame' is a single picture (snapshot).
 It is made up of many lines.
 Each frame has a synchronizing pulse (Vertical Sync).
 Each line has a synchronizing pulse (Horizontal Sync).
 Brightness is represented by positive voltage.
 Horizontal and Vertical intervals both have blanking.



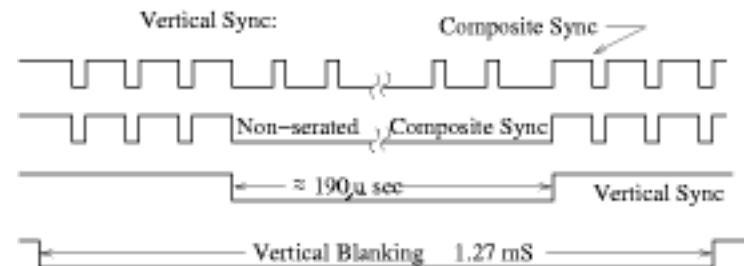
L17.3 Synchronization

The picture consists of white dots on a black screen.
 White is the highest voltage.
 Black is a low voltage.
 Sync is below the black voltage.
 Sync pulses are in the middle of the blanking interval.



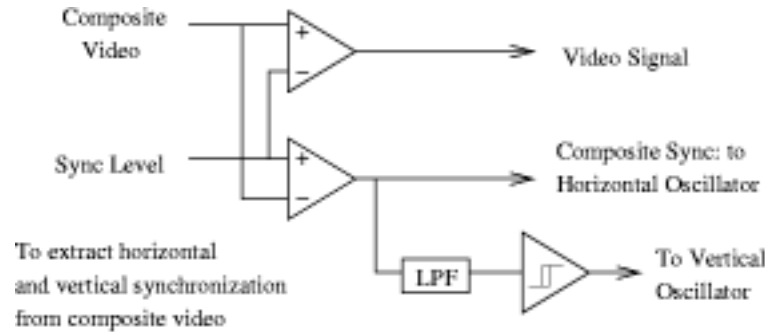
L17.4 Composite Synchronization

Horizontal Sync coordinates line.
 Vertical Sync coordinates frames.
 They are similar except for the time scales.
 And they are superimposed on one another.



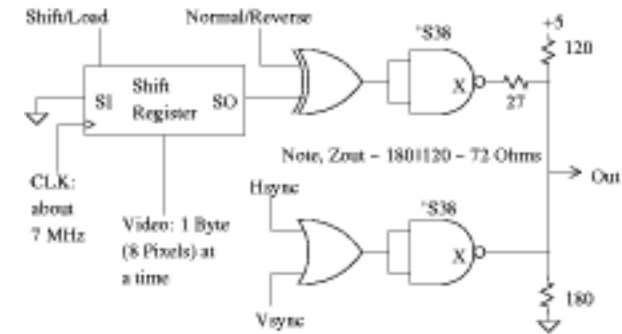
L17.5 Recovery of Signals (Conceptual)

Composite video has picture data and both syncs.
 Recovery is easy since the video is above the sync.
 Simple comparators extract video and composite sync.
 Composite sync is fed directly to the horizontal oscillator.
 Vertical sync is slower and a low-pass filter is used to separate it and then the signal is squared up by a Schmidt Trigger.



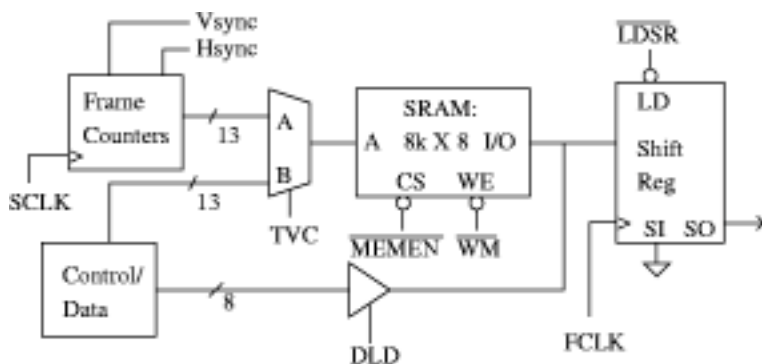
L17.6 Generation of Signals

This is a simple way of generating monochrome signals.
 This assumes one bit per pixel and also provides for reverse video.
 The output resistance is ~ 75 ohms.
 The 'S38 part is open collector so the voltages are determined by the resistor network.



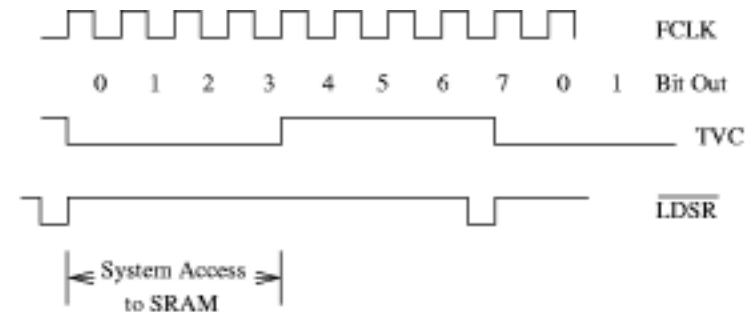
L17.7 Control

Here is one possible display format.
 256 pixels per row by 192 rows
 7.16 MHz clock => 140 nanoseconds per pixel
 Display time for the active line is 35.8 microseconds.
 256 x 192 = 48k pixels = 6 k bytes



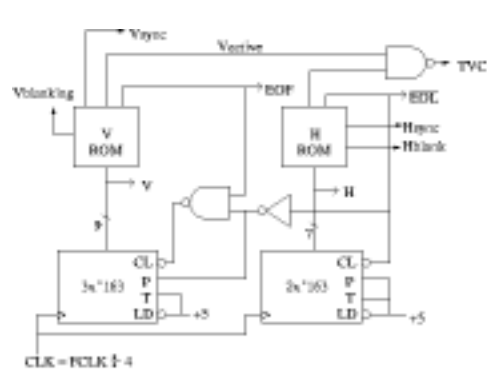
L17.8 Timing of Control Signals

Frame counters (including logic) produce sync signals.
 The shift register output is the video signal.
 TVC gives the shift register access half the time.
 LDSR (negative true) controls loading of the memory.
 DLD enables system data to the picture memory.



L17.9 Generation of Control Signals

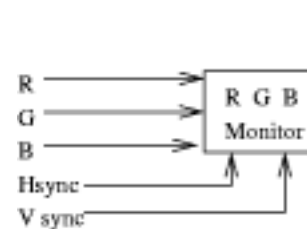
Here is one scheme for generating the control signals. Information can be stored in ROMs to generate sync signals, TVC, and /EOL. No external logic is needed if one prom is used by having V[7:0] as high bits of the ROM address and H[5:1] as the low bits of the ROM address.



Vertical ROM		
No. Words	Addresses	Contents
192	0 - 191	Vactive
26	192 - 217	Vblanking
6	218 - 223	Vsync
37	224 - 260	Vblanking
1	261	EOL
Horizontal ROM		
No. Words	Addresses	Contents
32	0 - 31	Hactive
9	32 - 40	Hblanking
7	41 - 47	Hsync
8	48 - 55	Hblanking
1	56	EOL

L17.10 Color Displays

Color displays are similar to three monochrome displays operated together, i.e., the colors add. Three binary video signals yield an eight color display. More colors are possible with more bits. Some monitors have an analog video input for each color. Sync is sometimes on a separate wire and sometimes is superimposed on the green signal.

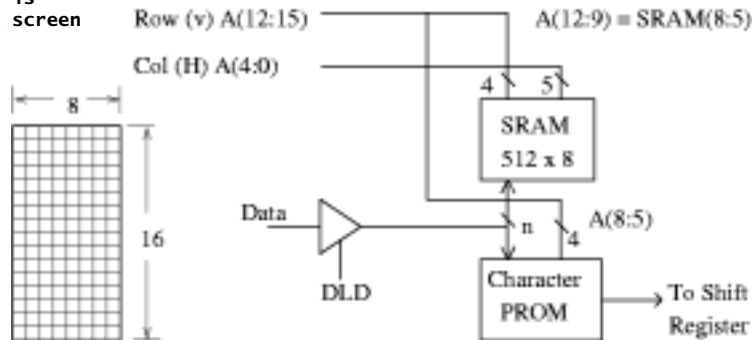


	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Purple	1	0	1
Yellow	1	1	0
White	1	1	1

L17.11 Character Displays (8 x 16 pixels)

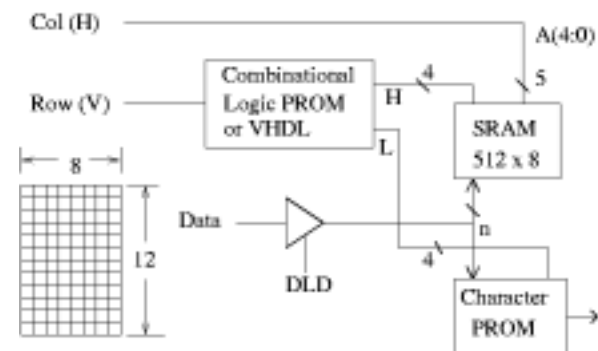
Characters are fixed bit patterns so always have the same shape, but can appear at different places on the screen. Use of characters can save video memory and also make the manipulation of video memory simpler.

The formatting is simple. For a screen of 256 pixels by 192 cols, one gets 384 characters. The screen address is used to specify the position and part of the address of the character PROM.



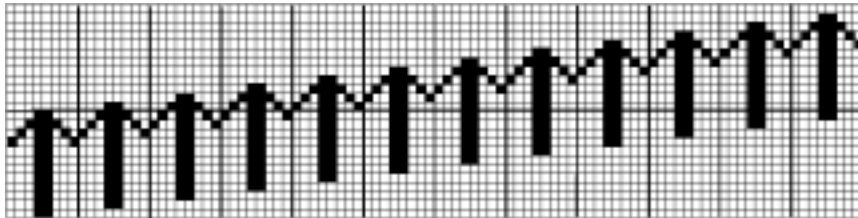
L17.12 Character Displays (8 x 12 Pixels)

The formatting is not as simple as before. However, re-mapping is done easily in a PROM or with VHDL. For a screen of 256 pixels by 192 cols, one gets 512 characters. As before, the screen address modified by the combinational logic is used to specify the position and part of the address of the character PROM.



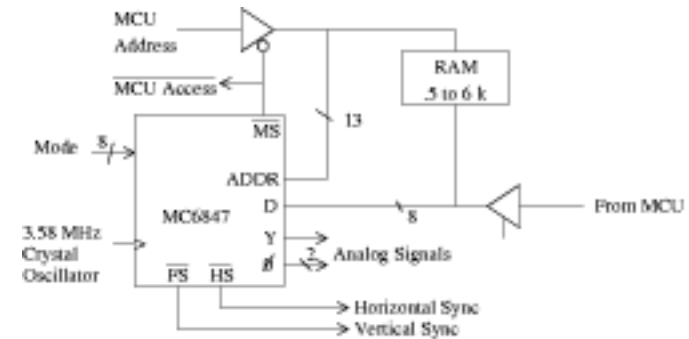
L17.13 Pairs of Characters

Sometimes, pairs of characters can create the same motion effect as bit-mapped graphics.
 The speed of the motion depends on the update rate.
 The following 24 characters can display an arrow at any vertical position.



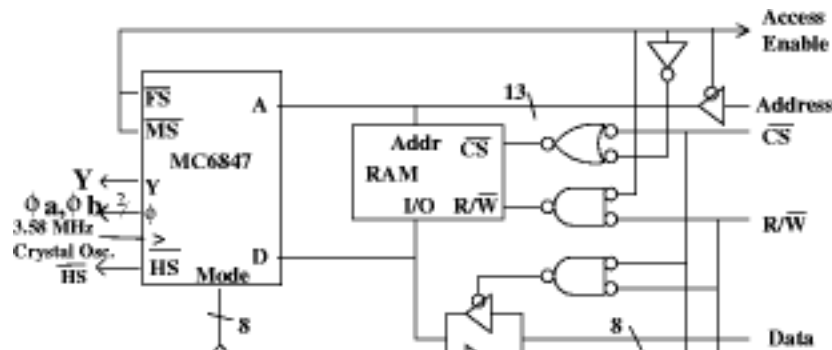
L17.14 Video Controllers

MC6847 is obsolete, but easy to use.
 It provides a 13-bit address and an analog video signal.
 It reads 8-bit data which can be a character code or video.
 Several display modes include 256 x 192 two color and several other color graphics with lower resolution.



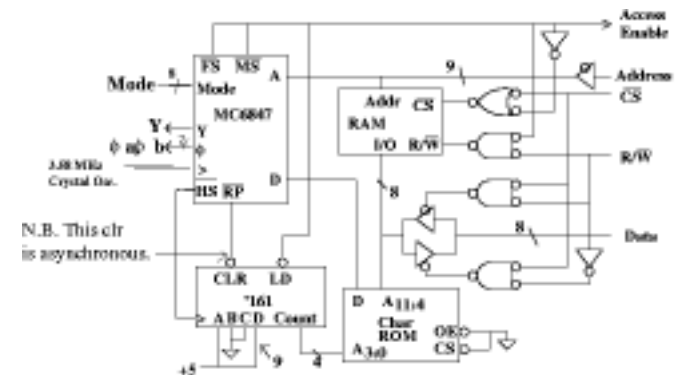
L17.15 Bit-Mapped Video

MC6847 can be used with bit-mapped video.
 Here is the digital system side.
 I will say more about Y, phi a, and phi b later.



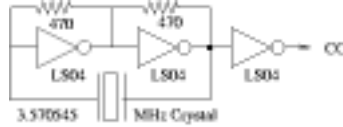
L17.16 MC6847 with a Character ROM

You can call it a bug or a feature.
 To get around the fact that /RP begins and ends between /HS, one must use a counter that has asynchronous clear, such as the '161. Of course, one can implement the counter with VHDL, but one has to remember to implement an asynchronous clear.

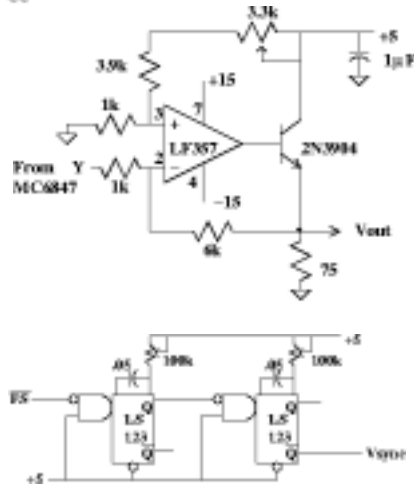


L17.17 Using the 6847

First, one must supply a clock to the MC6847.



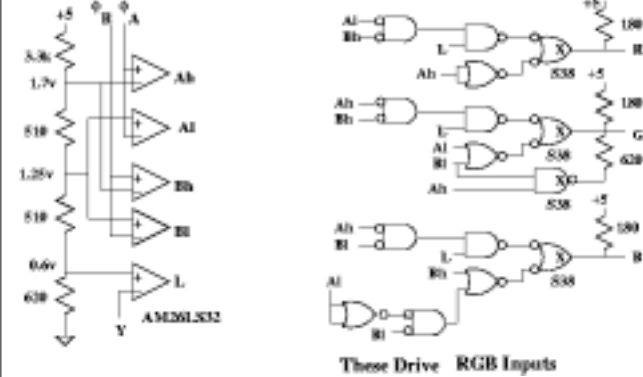
Here is a simple way of driving a monochrome monitor. Don't make the gain of the '357 too small or you will get some ringing. The Y output has composite sync and luminance.



The MC6847 generates blanking, not vertical sync. The first one-shot triggers on the falling edge of /FS and determines the delay of Vsync. The second one-shot determines the width of Vsync. Adjust the timing so that the picture is centered on the monitor.

L17.18 Color Output

For color output, one needs to decode the analog chroma signal and generate a digital color drive signal. The AM26LS32 is a "fast" comparator (it is actually a line receiver). The combinational logic can (should) be implemented in VHDL. The logic needed depends on the mode selected. Look at the Ah, Al, Bh, Bl, and L outputs to determine the logic needed. The 74S38 driving the 620 ohm resistor is needed if you want orange.



- The pinout of an available RGB cable is:
- Pin 1 Intensity
 - Pin 2 Red
 - Pin 3 Green
 - Pin 4 Blue
 - Pin 5 GND
 - Pin 6 GND
 - Pin 7 HSYNC
 - Pin 8 VSYNC

These Drive RGB Inputs