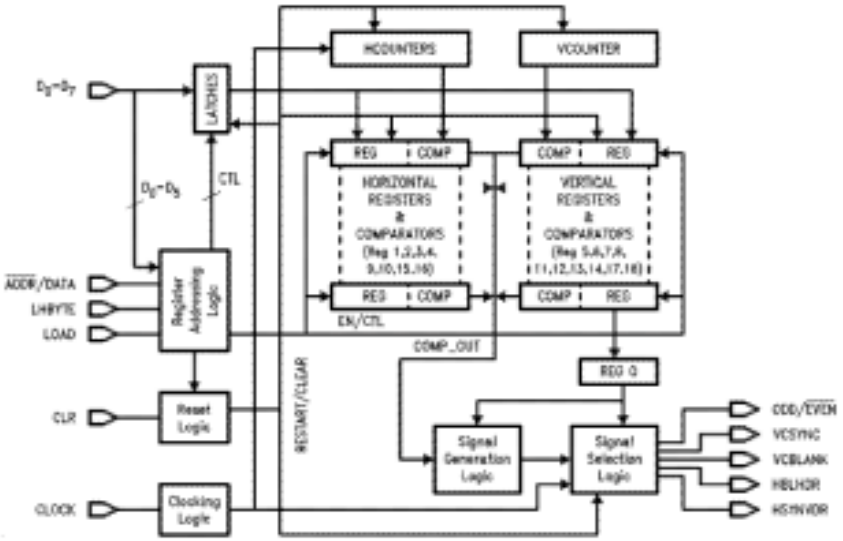
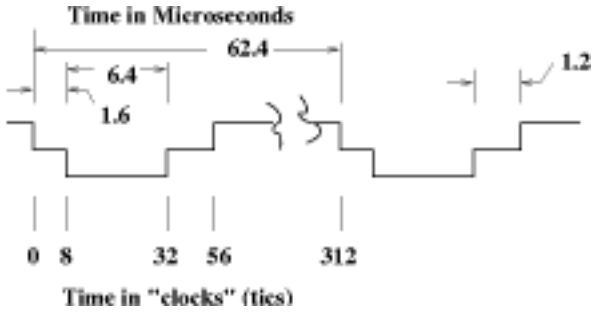
L18.1 LM1882 Sync Generator



L18.2 Sync Generator Example

LM1882 is flexible; timing information is stored in registers.
See data sheet no. 95 for particulars.
One example is:
- **256 pixels wide**
- **256 lines**
- **5 MHz clock (probably not typical)**



L18.3 Sync Generator: Register Contents

Register Contents:

Horizontal (Line) Control

R1	9	Horizontal Front Porch	} Time in "clocks"
R2	33	Horizontal Sync Pulse End	
R3	57	Horizontal Blanking	
R4	312	Line Width – must be even	

Vertical (Frame) Control

R5	4	Vertical Front Porch	} Lines
R6	7	Vertical Sync Pulse End	
R7	21	Vertical Blanking	
R8	276	Frame: 256 lines + 20 lines blanking	

Register 0: Contents 0110 0001 1000

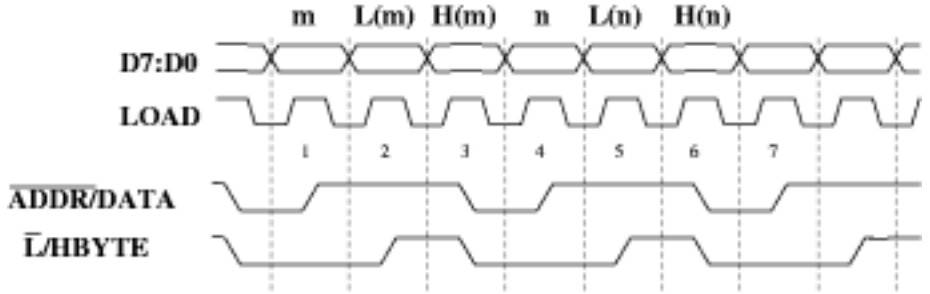
Bit 10: Enable System Clock	1
Bit 9: Disable Equalization	1
Bits 8:5 Sync Pulses Active Low	0000
Bits 4:3 Non–Interlaced	11
Bits 2:0 Default Output Config:	000

Pin 12 CBLANK, Pin 13 HGATE, Pin14 CSYNC, Pin 15 VGATE

L18.4 Sync Generator – Manual Mode

LM1882 must be loaded on power up.

Cycle No.	Load Falling Edge	Load rising edge
1	Enable Manual Addressing	Load address m
2	Enable Lbyte Data Mode	Load Lbyte m
3	Enable Hbyte Data Mode	Load Hbyte m
4	Enable Manual Addressing	Load address n
5	Enable Lbyte Data Mode	Load Lbyte n
6	Enable Hbyte Data Mode	Load Hbyte n

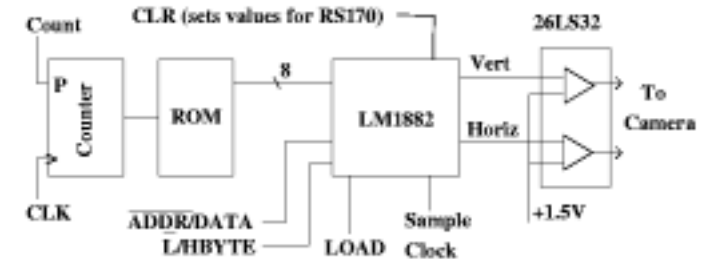


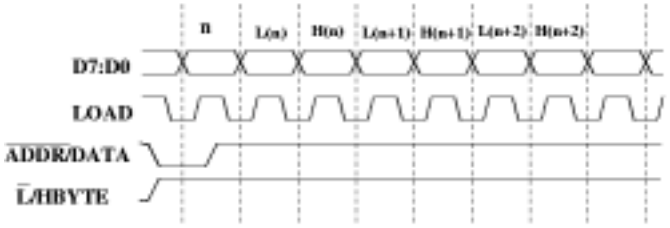
L18.5 Sync Generator − Automatic Mode

LM1882 must be loaded on power up.

Use a PROM to hold configuration register values.

Your MCU or FSM must do the programming.





L18.6 Sync Separator

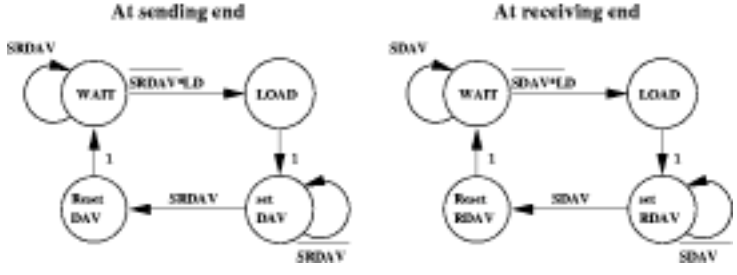
A sync separator operates in the reverse direction.
GS4981 generates composite sync from video.
It also generates separated sync signals.
However, your pixel clock must be synchronized with the recovered horizontal sync. If you do this synchronization with the pixel clock frequency directly, then the pixel clock used will "crawl" a whole pixel time. It is better to use a faster clock, say 4 times, to do the synchronization and then the "crawl" will only be 1/4 of a pixel time (distance).

L18.7 Getting Information form Here to There

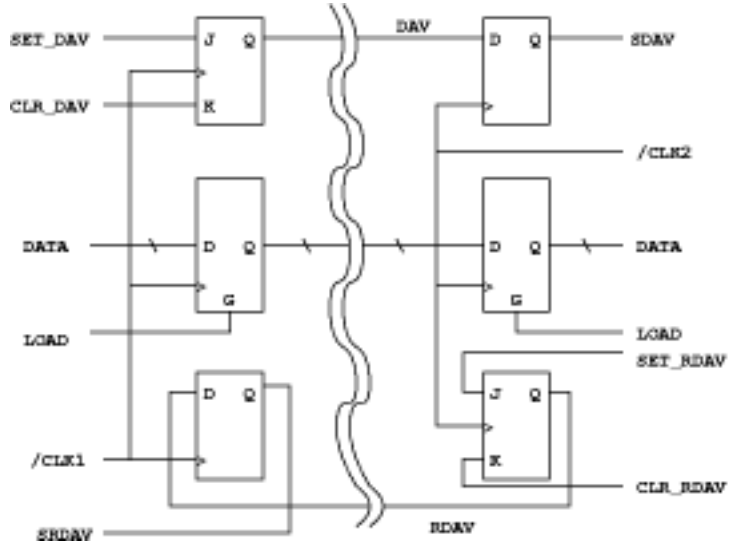
Full Handshake

Assumes "Here" and "There" have unrelated clocks such as might exist when the two locations are on separate kits.
It is always safe to assume this even when you are not sure.

* and we want to send more data, i.e, LD is true.



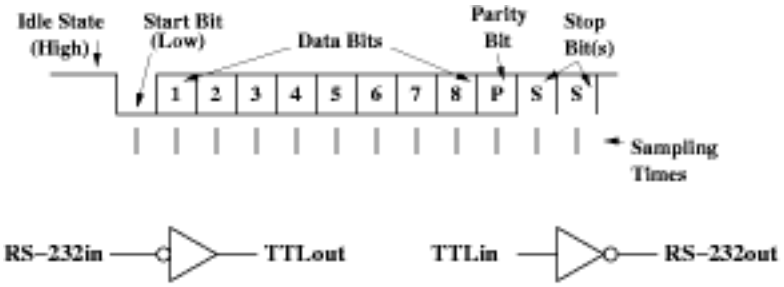
L18.8 Parallel Interface − Full Handshake



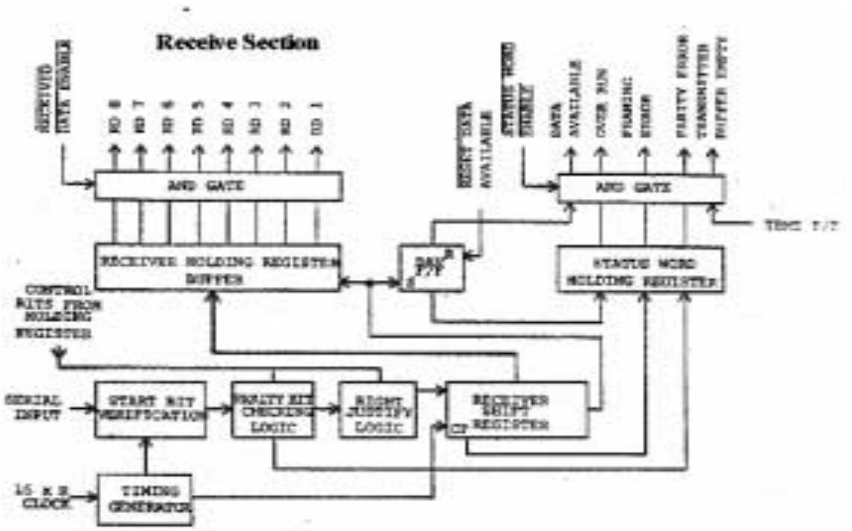
L18.9 Serial Interface

RS-232 is a serial interface standard.

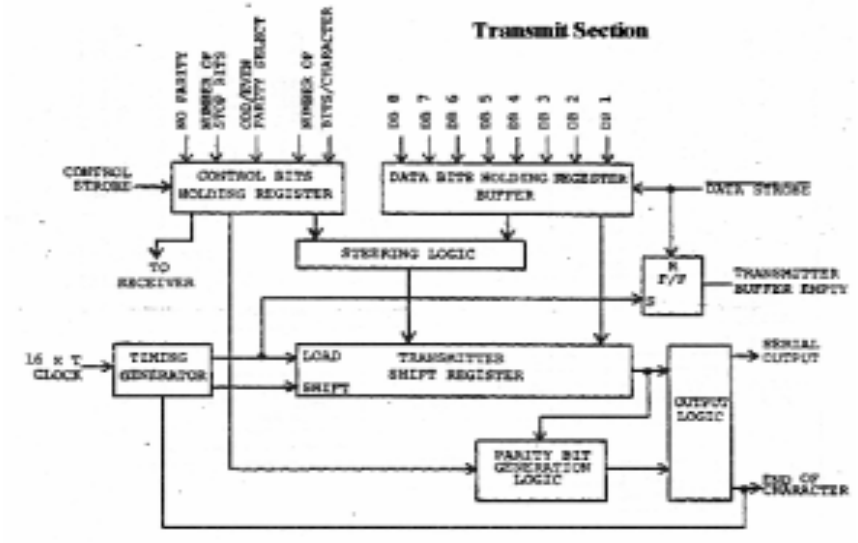
RS-232 levels are between -3v and -15v for a logic 1
and between +3v and +15v for a logic 0.
Shown below is the TTL signal, where the "idle" state is a logic 1.
The chip, MAX202, has 2 RS-232 to TTL and 2 TTL to RS-232 level converters.



L18.10 AY-3-1015D Receive Section



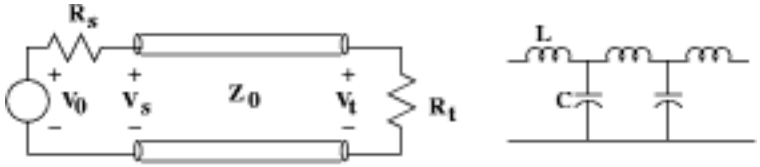
L18.11 AY-3-1015D Transmit Section



L18.12 Transmission Lines

Signals travel on wires

Have attenuation - losses
Have reflections - affected by terminations



Transmission Line has characteristic parameters:

L: Inductance per unit length
C: Capacitance per unit length

Z_0 : Characteristic Impedance

U_0 : Phase Velocity

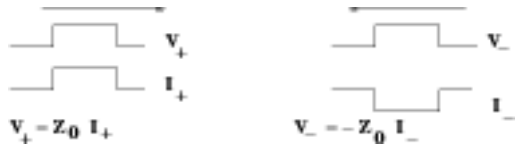
$$Z_0 = \sqrt{\frac{L}{C}}$$

$$U_0 = \sqrt{\frac{1}{L\,C}}$$

L18.13 Signal Propagation

Pulses traveling on the line

- Voltage and Current
- Ratio of voltage to current is 'characteristic impedance'
- Sign of that ratio is direction of propagation
- Propagate at < C (speed of light)



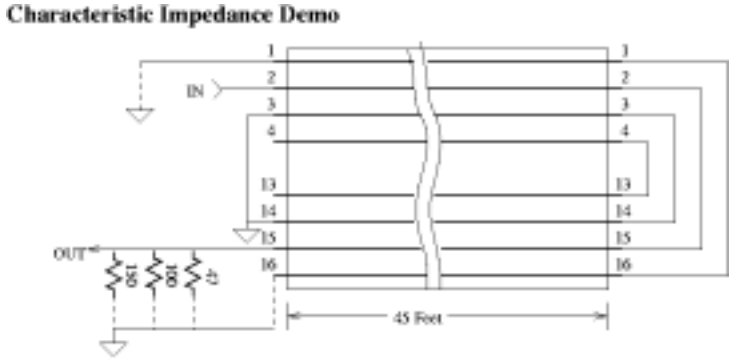
Pulses traveling on the line

- Voltage and Current
- Ratio of voltage to current is 'characteristic impedance'
- Sign of that ratio is direction of propagation
- Propagate at < C (speed of light)

L18.14 Characteristic Impedance Demo

Reflections depend on terminating impedance (resistance).

- Reflections can be minimized by terminating correctly.



Moral: Terminate Wires in Characteristic Impedance

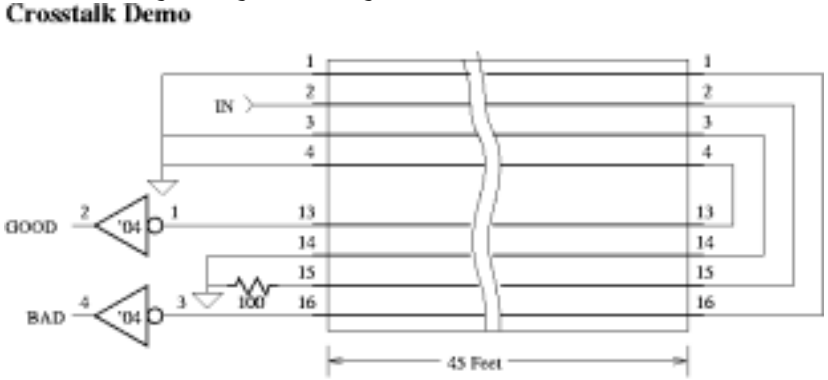
L18.15 Crosstalk Demo

Flat Ribbon Cable

- Similar to kit interconnect cables
- Wire situated next to each other
- Capacitive and inductive coupling

Crosstalk minimized by grounding alternating wires

- Ground - signal - ground - signal ...



Moral: Alternate Ground and Signal Wires in Cables