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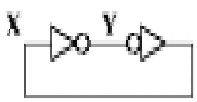
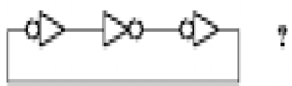
L4.1 Feedback Wed. February 13, 2002

Feedback produces 'State' which can be used to store information.



X	Y
0	1
1	0

Note that either state (X=0, Y=1 or X=1, Y=0) is valid.



Try this in the lab.

What does this one do?

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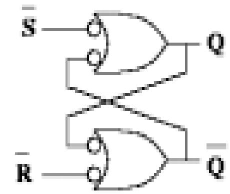
L4.2 Latch Wed. February 13, 2002

S–R Latch (74LS279)



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	1	0
		0	1

} Both work! (Holds state)

Question: What happens if $\overline{S}$ and $\overline{R}$ go 0 to 1 at the same time?

You can build a latch from NAND gates, but there is a packaged MSI version.
Question: What happens if you use NOR gates?

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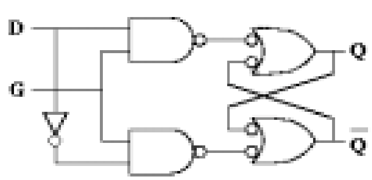
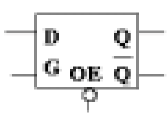
L4.3 D Latch Wed. February 13, 2002

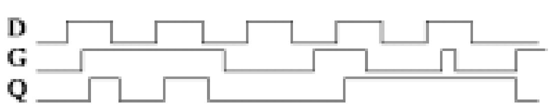
D Latch



74LS373 is an octal latch with tristate outputs.



The latch is a "follow and hold":



A latch is an important abstraction. Its input is controlled by a gate. When the gate goes from high to low, the state of the device holds.
Question: What happens if the gate and the input change state at nearly the same time?

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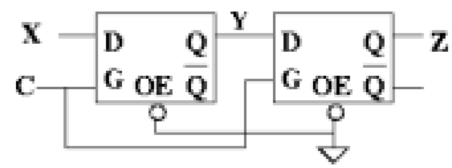
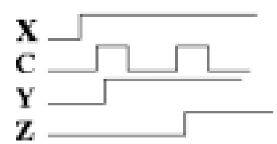
L4.4 Not a Shift Register Wed. February 13, 2002





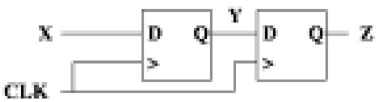
Will this do what we want?

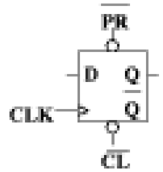
There is a problem with latches in multi–stage logic.
How many stages of logic will be affected by an input signal change during one clock cycle (G high)?

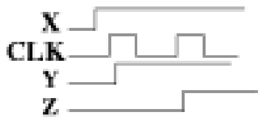
Multi–phase clocks can be used with latches (half the Gs high for one instance and the other half the next).
Another solution is to use an edge triggered flip–flop.

L4.5 Shift register — Wed. February 13, 2002

Edge triggered flip–flops can do what we want, namely, a shift register.

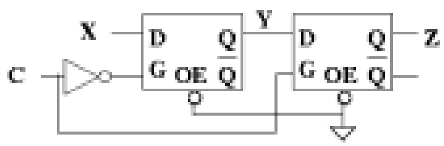




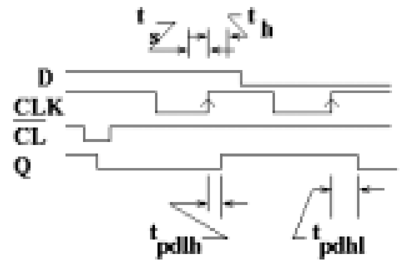


74LS74 has two of these. Preset and Clear are active low and asynchronous.

Edge triggered flip–flops can be implemented by a master slave arrangement of latches.



L4.6 Timing .Parameters — Wed. February 13, 2002



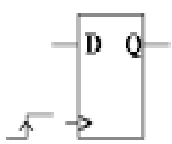
Typical Timing Parameters for 74LS Parts

Setup	t	≥ 20 nS
Hold	t	≥ 5 nS
Clock to Q		≤ 20 nS
CL or PR to Q		≤ 25 nS
CLK high		≥ 25 nS
Max Frequency		25 MHz

Setup time: Input must be stable before the clock rising edge.
Hold time: Input must stay stable after the clock rising edge.
Clock to Q: Maximum time for the output to be stable after the clock edge
CL or PR to Q: Maximum time for the output to be stable after an asynchronous input assertion
Contamination time: Minimum time until an output changes from the clock edge or an asynchronous input assertion – hardly ever specified!
Max Frequency = 1(Clock HIGH + Clock LOW)

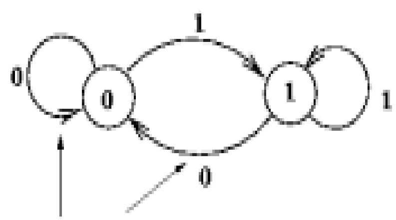
L4.7 D and T Flip−Flops — Wed. February 13, 2002

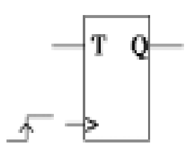
Flip–flops are simple finite state machines which have two–states.



D Flip–Flop

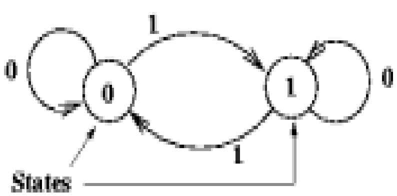
D	Q_n
0	0
1	1



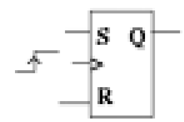


T Flip–Flop (toggle)

T	Q_n
0	Q_{n-1}
1	$\overline{Q_{n-1}}$

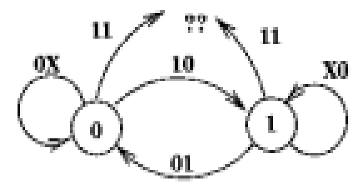


L4.8 SR and JK Flip−Flops — Wed. February 13, 2002

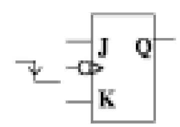


S–R Flip–Flop

S	R	Q_n
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	?? ← Undefined State!

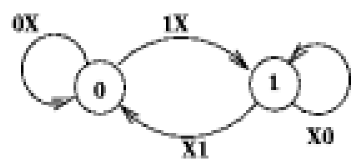


The SR flip–flop is an edge triggered version of the SR latch. It has an undefined state problem which is resolved by the JK flip–flop.



J–K Flip–Flop

J	K	Q_n
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	$\overline{Q_{n-1}}$



Note that this version of the JK flip–flop has a negative edge triggered clock as indicated by the bubble.

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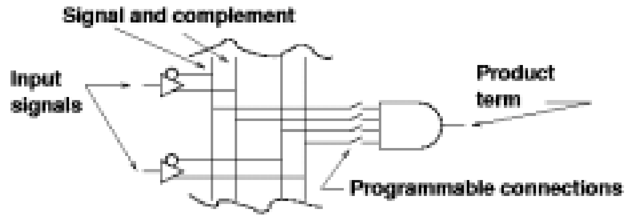
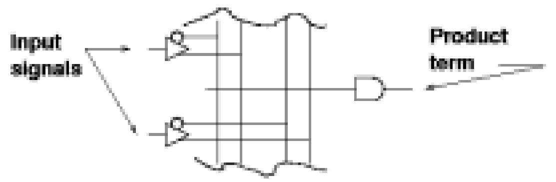
L4.9 Programmable Logic — Wed. February 13, 2002

The basic element of all PALs (PLDs and CPLDs) is an AND gate which can be driven by each input and its complement. The unprogrammed state is that all connections are intact; therefore, the product term is zero. When all connections are destroyed (temporarily) the output of the AND floats high and is thus a one.



A shorthand notation (especially useful if there are a lot of inputs) is:



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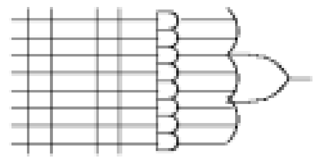
L4.10 OR of ANDs — Wed. February 13, 2002

The product terms produced by the ANDs are combined in large ORs.



And the output from the OR can usually be registered or simply . combinational. Additionally, either can be inverted or not.

Pin	20V8(1) Use	20V8(1) Terms	20V8(2) Use	20V8(2) Terms*	22V10 Use	22V10 Terms
23	I		I		I/O	8
22	O	7	I/O	8	I/O	10
21	I/O	7	I/O	8	I/O	12
20	I/O	7	I/O	8	I/O	14
19	I/O	7	I/O	8	I/O	16
18	I/O	7	I/O	8	I/O	16
17	I/O	7	I/O	8	I/O	14
16	I/O	7	I/O	8	I/O	12
15	O	7	I/O	8	I/O	10
14	I		I		I/O	8
13	I		/OE		I	

20V8 (1): All outputs are combinatorial (none registered).
(2): Some outputs registered: 8 product terms for registered outputs only.

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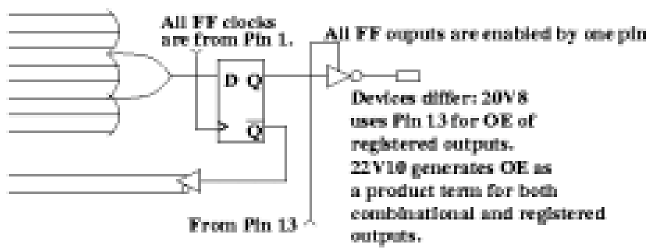
L4.11 Outputs — Wed. February 13, 2002

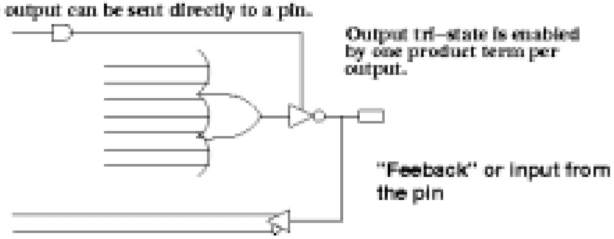
This is how the 20V8 works.

The output can be registered.



Devices differ: 20V8 uses Pin 13 for OE of registered outputs. 22V10 generates OE as a product term for both combinational and registered outputs.

The output can be sent directly to a pin.



Output tri–state is enabled by one product term per output.

"Feeback" or input from the pin

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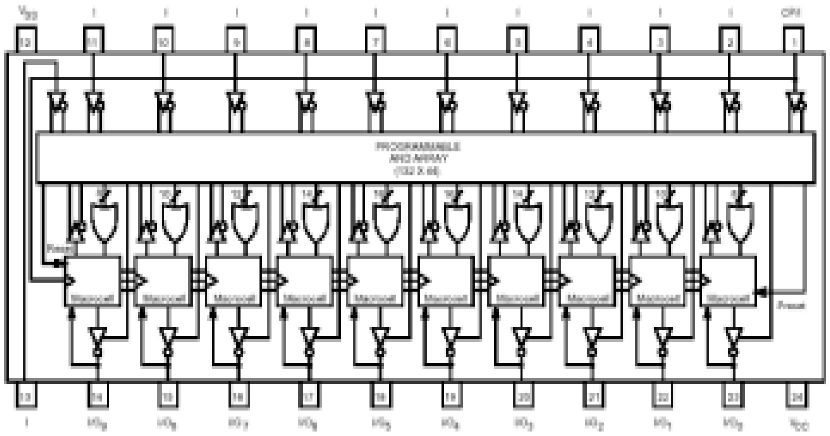
L4.12 Levels — Wed. February 13, 2002

PALs are CMOS, voltage levels are compatible with TTL.

	20V8	22V10	TTL(74LS00)
V_{OL}	0.5 V	0.4 V	0.4 V
V_{IL}	0.8 V	0.8 V	0.8 V
V_{OH}	2.4 V	2.4 V	2.7 V
V_{IH}	2.0 V	2.0 V	2.0 V
I_{OL}	24 mA	16 mA	8 mA
I_{OH}	–3.2 mA	–3.2 mA	–.4 mA
I_{IL}	-10 μA	-10 μA	–.4 mA
I_{IH}	-10 μA	-10 μA	20 μA

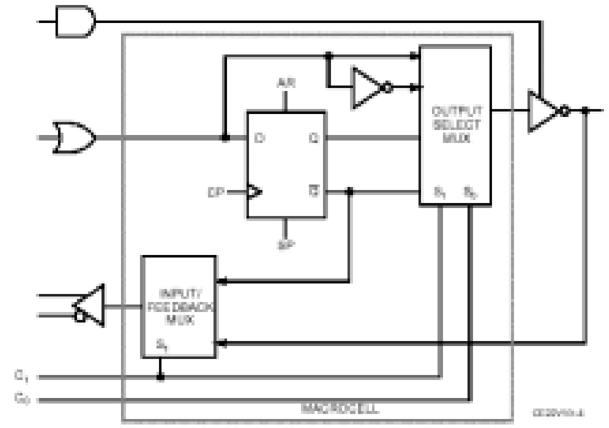
L4.13 22V10 Pal Wed. February 13, 2002

Flexible 'Macrocells'
10 Macrocells, varying number of product terms
The clock is still from pin 1.

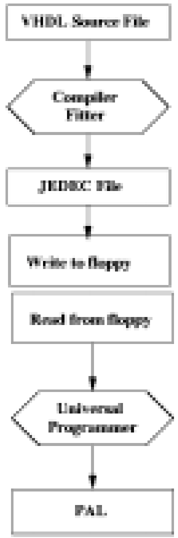


L4.14 22V10 Macrocell Wed. February 13, 2002

Flexible 'Macrocells'
10 Macrocells, varying number of product terms
The clock is still from pin 1.



L4.15 Programming Small PALs Wed. February 13, 2002

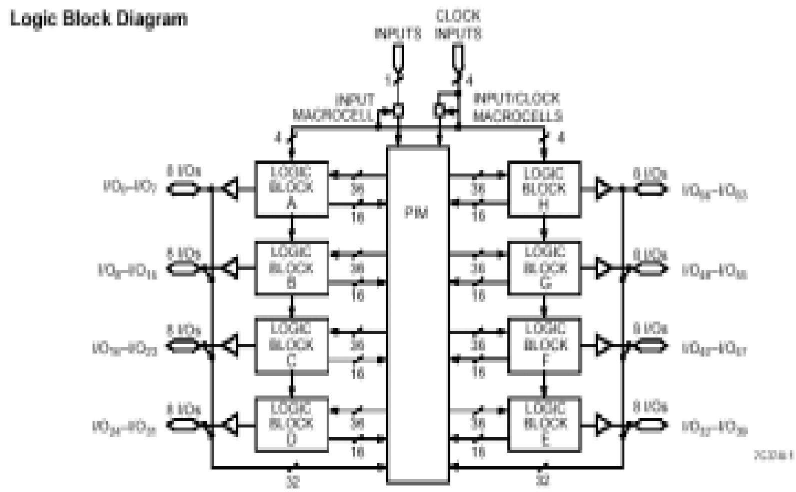


L4.16 CY7C374i Wed. February 13, 2002

Manufacturer is Cypress (URL is http://www.cypress.com).
Information about the 370 family and the data sheet for the CY7C374i are on the web page.
CPLDs are just more complicated PLDs.

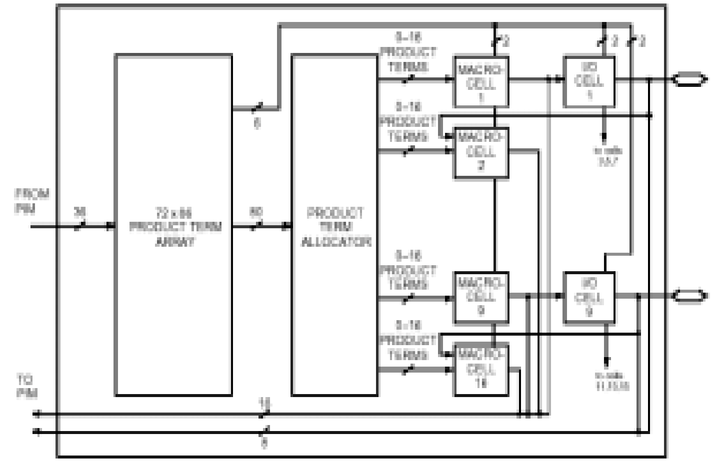
128 macrocells in eight blocks
64 I/O pins
5 dedicated inputs including 4 clocks
which are not usable on the 6.111 CPLD board
JTAG interface − ISR − In−System Reprogrammable
High Speed
fmax = 125 Mhz
tPD = 10 ns
tS = 5.5 ns
tCO = 6.5 ns

L4.17 CY7C374i Block Diagram Wed. February 13, 2002

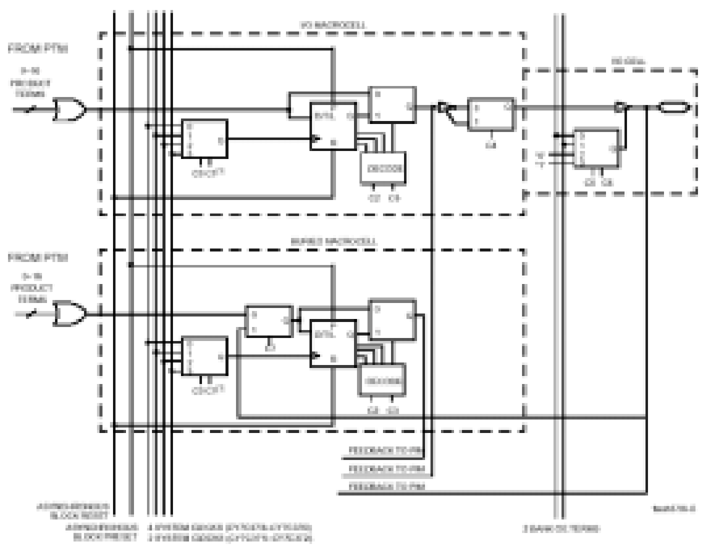


L4.18 CY7C374i Logic Block (1 of 8) Wed. February 13, 2002

Note that there are I/O and buried macrocells.

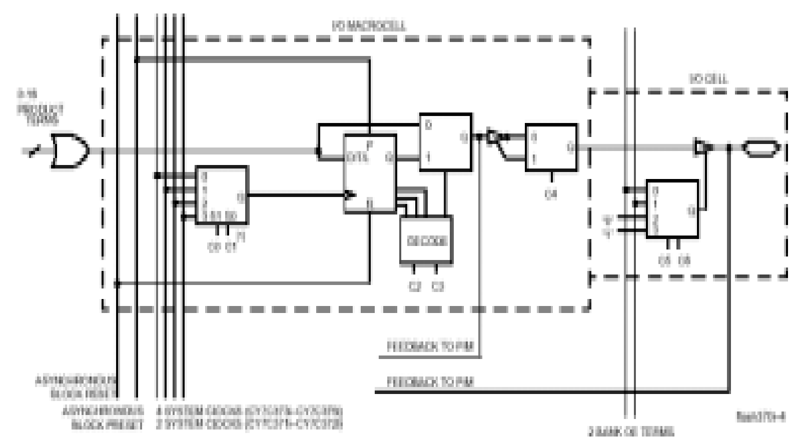


L4.19 CY7C374i Macrocells Wed. February 13, 2002

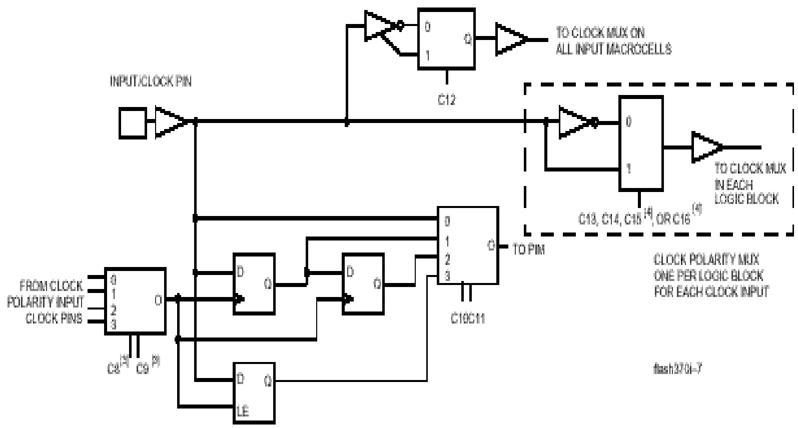


L4.20 I/O in More Detail Wed. February 13, 2002

Note that this is similar to the 22V10.



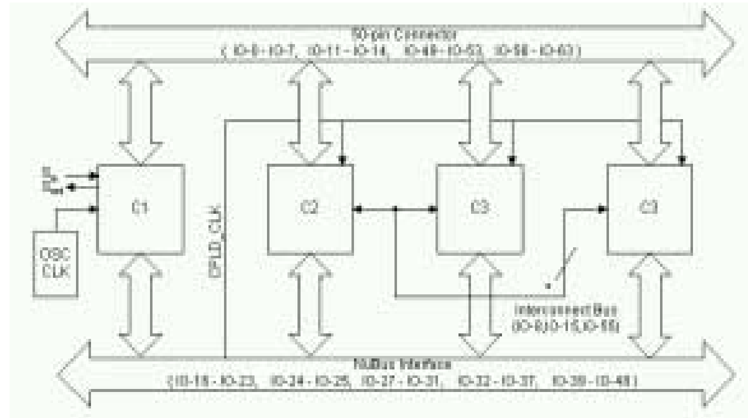
L4.21 CY7C374i Input/Clock Pins Wed. February 13, 2002



L4.22 CPLD Board Wed. February 13, 2002

Four CYPRESS 374i CPLDs which have 128 Macrocells

- The speed is 66 Megahertz. (Much faster than we can use!)
- CPLD pins are accessible via the AD bus and an optional 50 pin cable.
- Interconnections between chips limit the flexibility of signal allocation.



L4.23 CPLD Board (more) Wed. February 13, 2002

BEWARE! Some signals are grounded on the kit.

- Three CPLDs are clocked by one clock (AD31).
- The left CPLD can be used as an RS−232 interface via the DB−9 connector (although it need not be).

Jumpers select

- Which CPLDs will be programmed via the JTAG interface.
- 1.843 Mhz crystal as clock for the left hand CPLD.

It can be clocked by a buffered version of the clock supplied to the other CPLDs.