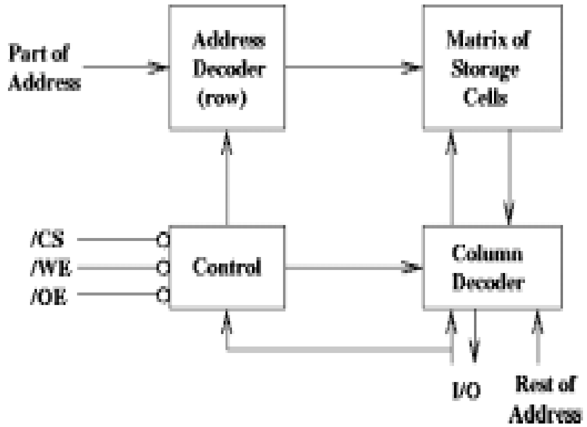
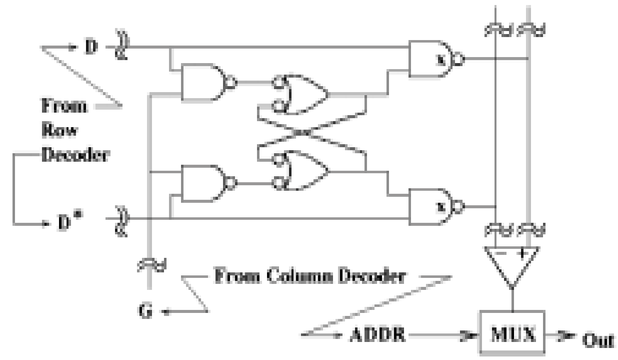
L8.1 Memory Fri. February 22, 2002

Memories are usually organized as two−dimensional arrays of cells.
The address is split into two parts, e.g., 64 kbits might have 16 address bits split into eight bits each for row and column addresses.



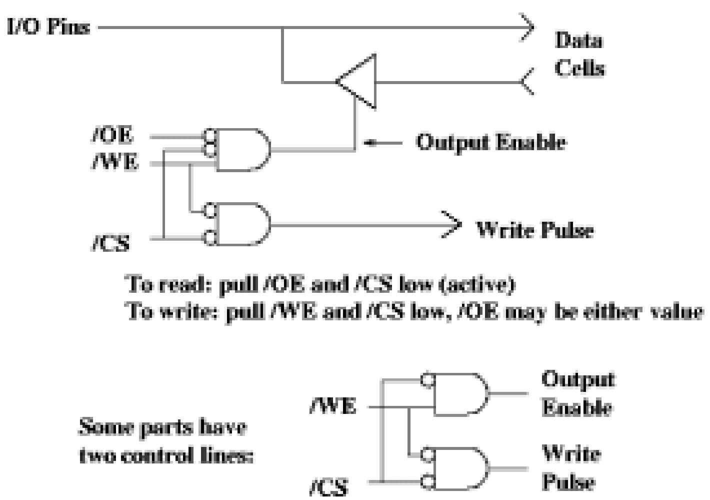
L8.2 Conceptual Memory Cell Fri. February 22, 2002

This is conceptually what goes on at the intersection of each row and column of the storage matrix. The function of one of these cells is present for each bit of storage.
A READ of the information stored is accomplished by setting D = D* = 1 so that the open collector gate pulls down one of the sense lines. If D = D* = 0 some other row is read.
A WRITE of information is accomplished by setting D = /D* and controlling G to be 1 for a time. The data is stored in the latch when G returns to 0.



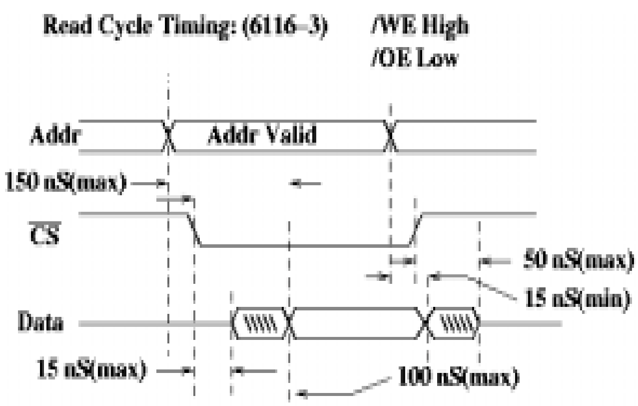
L8.3 Control Lines Fri. February 22, 2002

The control lines are often active low. One must read the data sheet.



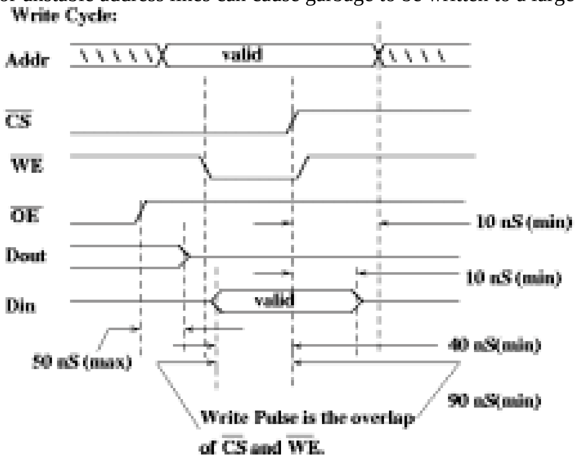
L8.4 Read Timing Fri. February 22, 2002

Data is output in response to chip select. At first, data is invalid; then the stored data is output 150 ns after the address is stable.
Note that data is still valid for 15 ns after the address changes (hold time).



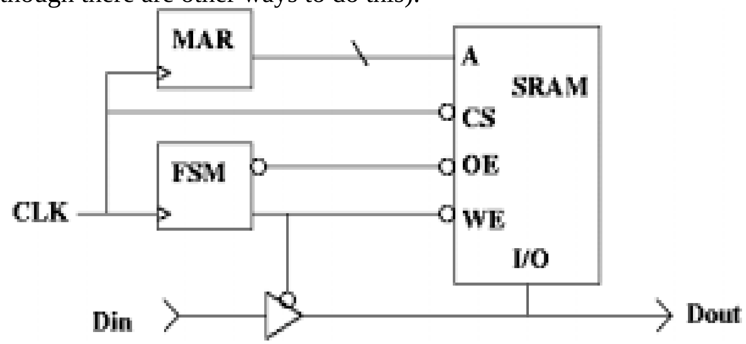
L8.5 Write Timing Fri. February 22, 2002

Write cycle timing is a bit more complex.
It is important that Address must be valid during the whole write pulse.
Data must also be valid for some time after the write pulse.
Tri−stated or unstable address lines can cause garbage to be written to a large number of locations!



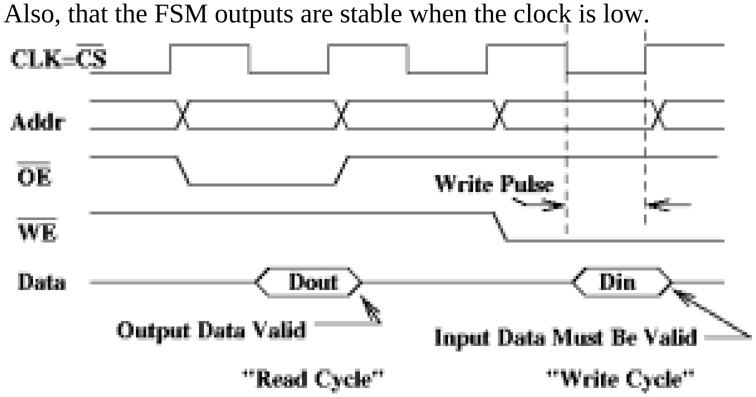
L8.6 A Possible Control Structure Fri. February 22, 2002

Here is a suggestion for controlling a memory with an FSM.
Tying CLK directly to /CS gives the FSM control signals time to settle
(for half the clock period) before they are "used" by the memory.
This helps to eliminate the possibility of bus contention
(although there are other ways to do this).



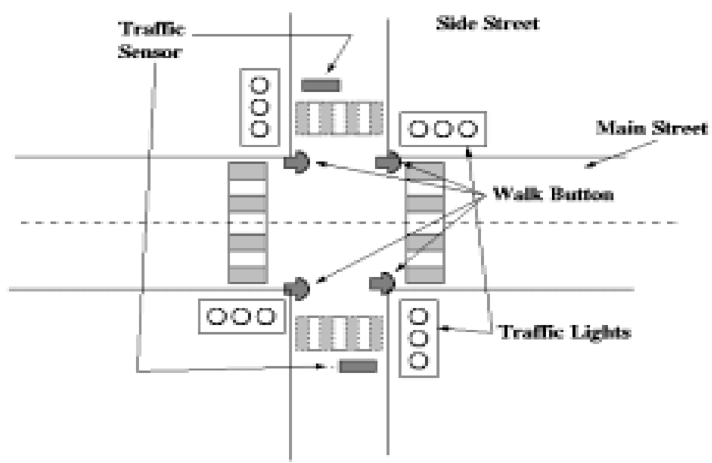
L8.7 Timing Diagram Fri. February 22, 2002

This timing diagram illustrates the scheme on the previous slide .
It assumes the address changes after the positive going clock edge and
is thus stable when the clock is low.
Also, that the FSM outputs are stable when the clock is low.

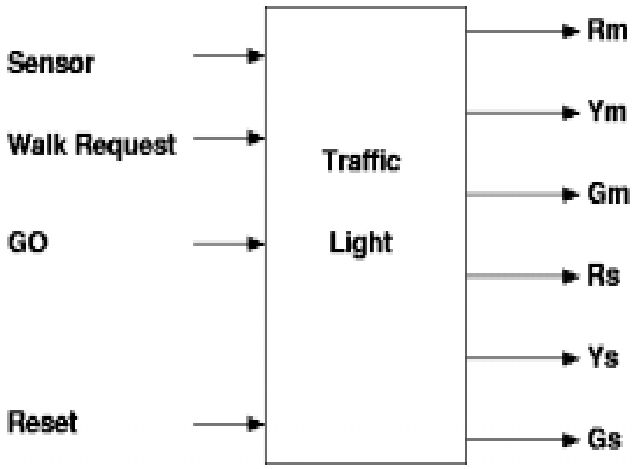


L8.8 Lab 2 Assignment Fri. February 22, 2002

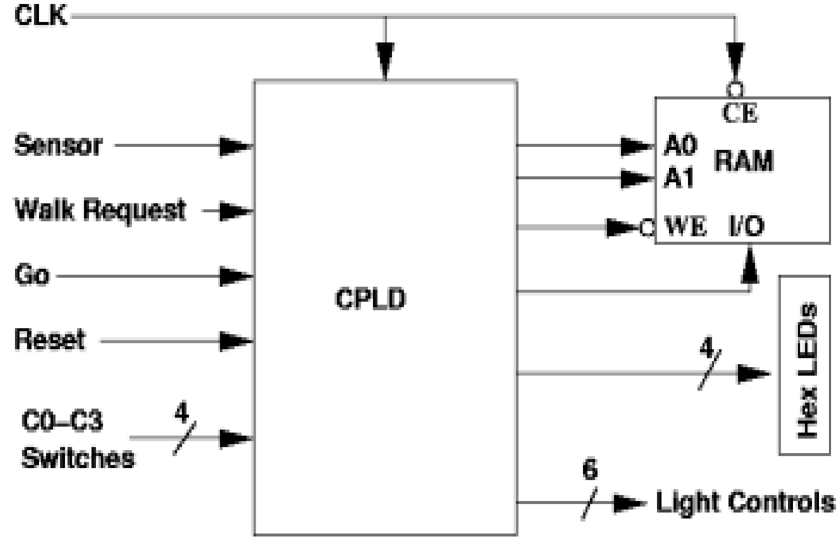
Traffic Light Controller



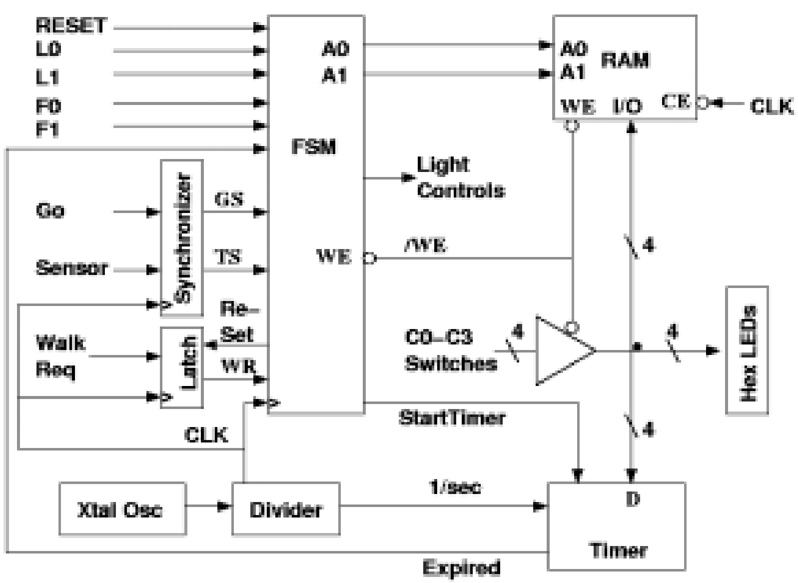
L8.9 Top Level Block Diagram Fri. February 22, 2002



L8.10 Implementation Details Fri. February 22, 2002



L8.11 Detailed Functional Diagram Fri. February 22, 2002



L8.12 Inputs to your FSM Fri. February 22, 2002

RESET	**(from a switch)**
GOSYNC	**(from Synchronizer)**
F1, F0	**Function Selection (from switches)**
L1, L0	**RAM Address**
Sensor	**Traffic Sensor (synchronized from a switch)**
WR	**Walk Request (Re−settable latch from pushbutton)**
EXPIRED	**Signal that timer has timed out**

Outputs From Your FSM

A1, A0	**SRAM Address**
WE	**SRAM Write Enable (source of bus signal)**
StartTimer	**Resets one second increment timer**
Gm, Ym, Rm, Gs, Ys, Rs	**Traffic light control signals**

L8.13 Inputs to your FSM Fri. February 22, 2002

Here are the functions your controller must implement:

F1 F0	are the function control switches
0 0	**Examine Memory Location Specified by Switches**
0 1	**Store Value in Memory Location Specified by Switches**
1 0	**Run Traffic Lights**
1 1	**Blink**

And for writing to or examining memory (functions 0 and 1) you should use these addresses:

A1 A0		
0 0	**TYEL**	**Time for yellow light**
0 1	**TBASE**	**Base interval**
1 0	**TEXT**	**Extension interval**
1 1	**TBLINK**	**Blink interval**

L8.14 Lab 2 Phase II Schedule Fri. February 22, 2002

There is an added step which is optional.

Feb. 22: Lab assignment (done today)

Feb. 26: Lab 2 design due (oral)

Mar. 8: Lab 2 checkoff (working hardware)

Mar. 11: Lab 2 report due

Mar. 14: Revised report due for students using Lab 2 as their phase II paper