

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

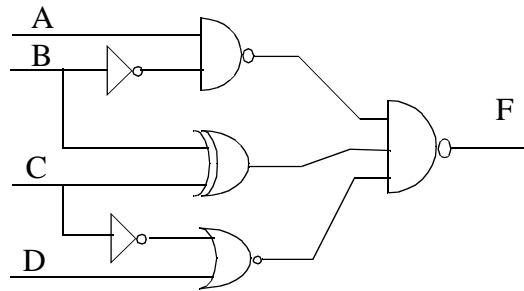
6.111 - Introductory Digital Systems Laboratory
Problem Set # 2

Issued: February 13, 2002

Due: February 20, 2002

Problem 1: Fun with Combinational Logic!!!

(a) Write the equation for the output of the circuit shown below. Using boolean algebra, simplify the equation until it is expressed in Sum of Products form. The expression does not have to be minimal.



(b) Build a truth table for the function F, using A as the most significant bit and D as the least significant bit.

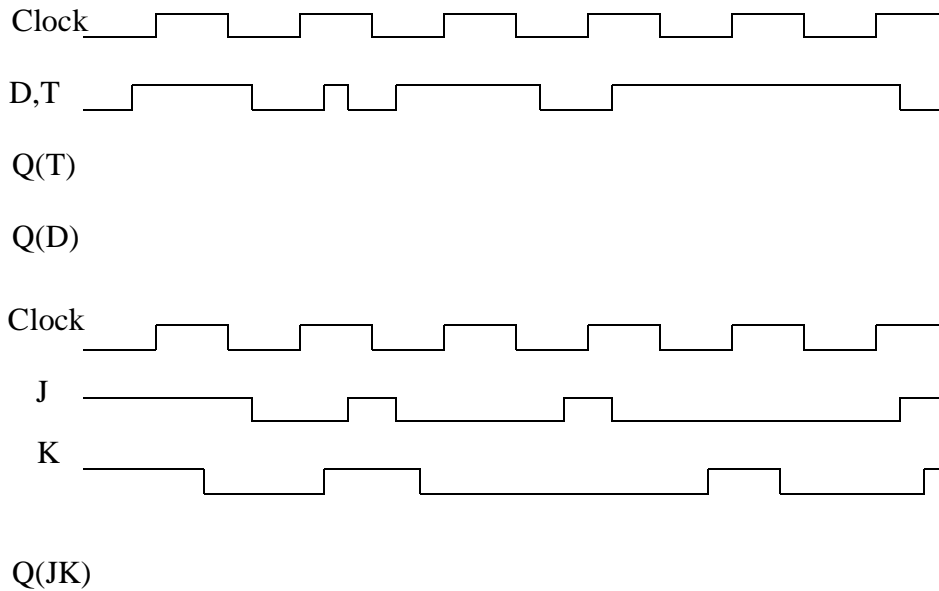
(c) Show the Karnaugh map for the circuit. Circle appropriate groupings to find a minimal sum of products expression.

(d) Is the MSP expression from (c) unique? Is it hazard free? If the expression has hazards, write a new expression that is hazard free.

(e) Write a short VHDL file that implements function F. Use a clocked process to latch the output so that the changes in the output will be reflected only on the rising edge of a clock signal.

Problem 2: Thou shall know his Flip-Flops!!!

Using the following timing diagram, draw the output Q (assuming Q starts at 0) for a negative-edge-triggered D flip-flop, positive-edge triggered T flip-flop, and positive-edge triggered JK flip-flop.

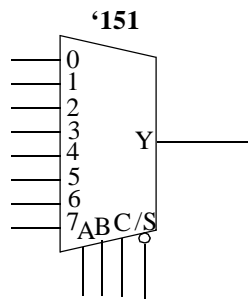


Problem 3: Multiplexers are your Friends

Write out the truth table for the following equation, using W as the most significant bit and Z as the least significant bit.

$$F = W / X / Z + / W X / Y Z + W Y + / X Y + Y / Z$$

Implement the function using an 8-to-1 multiplexer (mux), shown in the following diagram. Use W, X, and Y for the control leads with W acting as the most significant bit. The function can be generated by tying the remaining inputs to the mux to Z, /Z, 0, or 1. Label your diagram carefully, making sure that every input lead of the mux is connected with some input signal.



Problem 4: Counters are Crucial

(a) The '163 is a synchronous counter while a '393 is a ripple counter. What does this mean? Comment on their differences (design, performance, area, etc).

(b) There are multiple ways to create an 8-bit counter from two '163 chips. One might think to wire the RCO of the first counter into the clock input of the next counter, but it is a bad way of cascading two counters. Why? What is a better way of cascading two '163 counters?

(c) The crystal oscillator included in your lab kit cycles at a frequency of 1.8432 MHz. Draw a circuit that uses as many '163s (four-bit binary counters) as necessary to divide the signal from the crystal oscillator by 1,843,200 to achieve a one-second clock. Be sure to clearly label which output bit is the one-second output. Don't worry about trying to achieve a 50% duty cycle.

(d) Code the design from (c) in VHDL using bottom-up hierarchy. First create a VHDL file that emulates the '163 counter. After you have verified its functionality, add your logic to a top level VHDL file while instantiating the '163 counter model.