

Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science  
6.111 - Introductory Digital Systems Laboratory

**Quiz 1**

March 1, 2002

- 1 .....(20)
- 2 .....(20)
- 3 .....(30)
- 4 .....(30)
- TOTAL .....(100)

NAME .....

Indicate Your Section

- James Oey      12 PM
- Rajul Shah      1 PM
- Cynthia Chow      2 PM
- Jennifer Maurer      3 PM

This quiz is **Closed Book**: One handwritten “crib” sheet is allowed.

Put your name on all sheets and indicate your section on this page.

Write all your answers directly on the quiz.

Show all of your work.

You are not required to use a logic template, but you must **make sure your answers are legible**.

**Problem 1** (20 points)

		<b>ab</b>			
		<b>00</b>	<b>01</b>	<b>11</b>	<b>10</b>
<b>cd</b>	<b>00</b>	<b>1</b>	<b>0</b>	<b>1</b>	<b>0</b>
	<b>01</b>	<b>1</b>	<b>X</b>	<b>X</b>	<b>1</b>
	<b>11</b>	<b>1</b>	<b>0</b>	<b>1</b>	<b>1</b>
	<b>10</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>

Figure 1a

		<b>ab</b>			
		<b>00</b>	<b>01</b>	<b>11</b>	<b>10</b>
<b>cd</b>	<b>00</b>	<b>1</b>	<b>X</b>	<b>1</b>	<b>1</b>
	<b>01</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>1</b>
	<b>11</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>
	<b>10</b>	<b>1</b>	<b>X</b>	<b>0</b>	<b>1</b>

Figure 1b

A. Show groupings of the Minimal Sum of Products for the Kmap of Figure 1a.

B. Does this grouping exhibit a static hazard?

\_\_\_\_\_ yes      \_\_\_\_\_ no

If yes, then what additional product term should be included to eliminate this hazard?

C. What is the algebraic equation for groupings shown in Figure 1b?

D. Is the grouping minimal?

\_\_\_\_\_ yes      \_\_\_\_\_ no

If no, why not?

**Problem 2** (20 points)

A simple FSM is made of two D flip-flops, a NOR gate and a NAND gate, as shown in Figure 2.

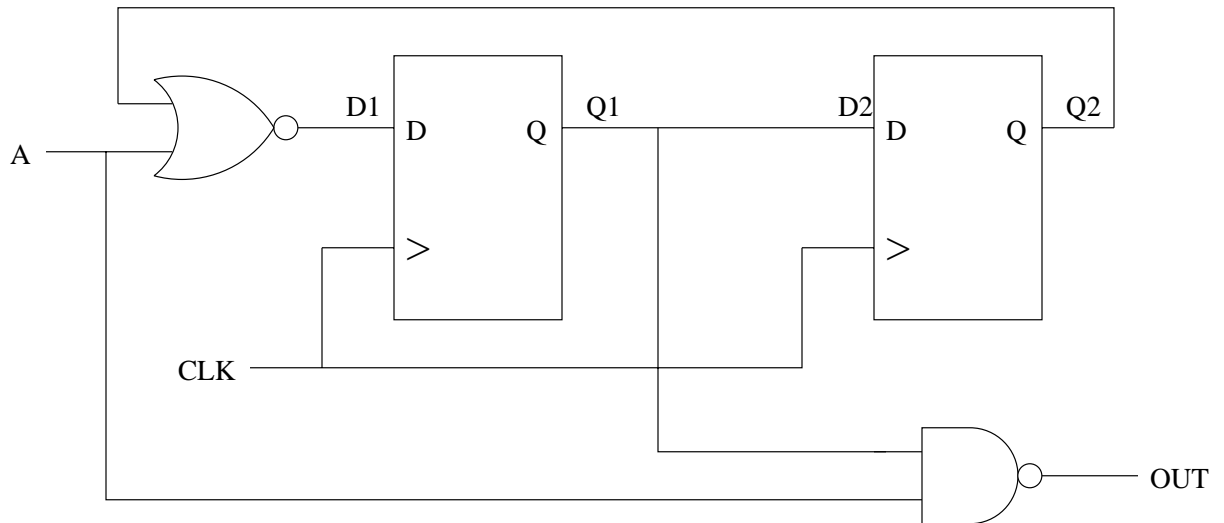
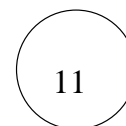
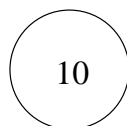
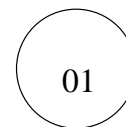
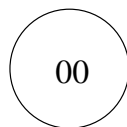


Figure 2

Draw a state transition diagram showing the states  $Q_1Q_0$ , and the transitions between the states. Use the template shown below. Note that the states are labeled such that 01 means  $Q_1 = 0$  and  $Q_0 = 1$ .



**Problem 3** (30 points)

A logical circuit with two flip-flops is shown in Figure 3a. Assume that the input signal **IN** has been HIGH for long enough that everything is in the 'steady state'. Finish the timing diagram shown in Figure 3b. Assume that all gate and register delays are short enough compared with the clock period that they can be ignored here. Note, Qa is the LSB.

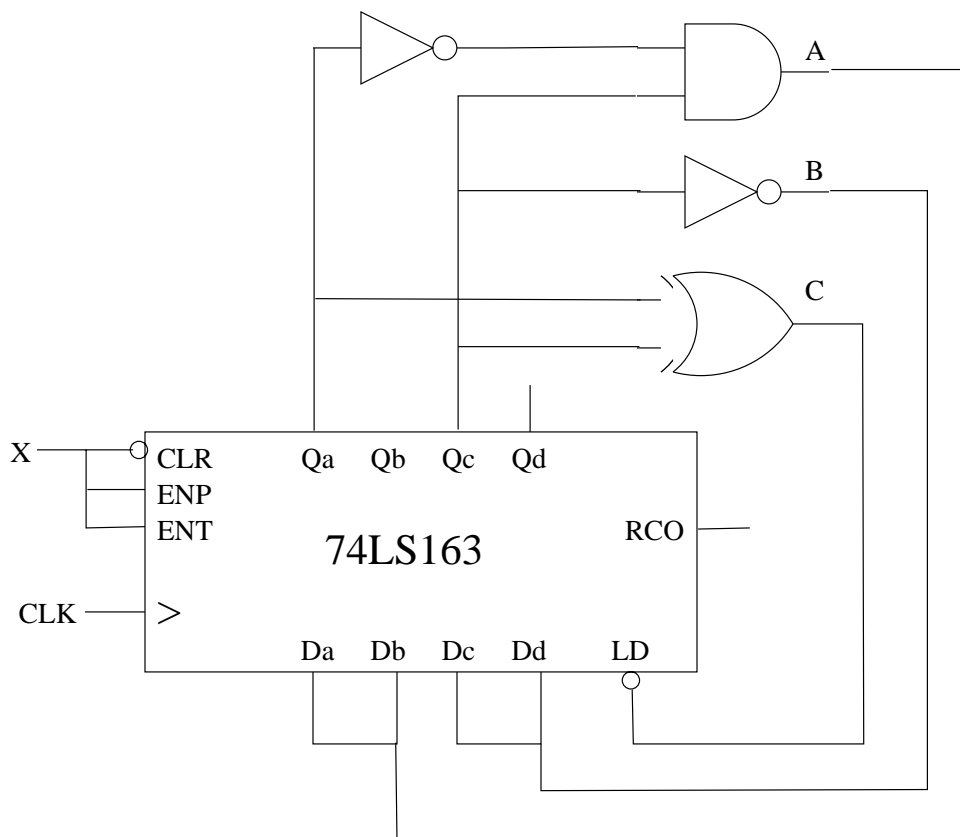


Figure 3a

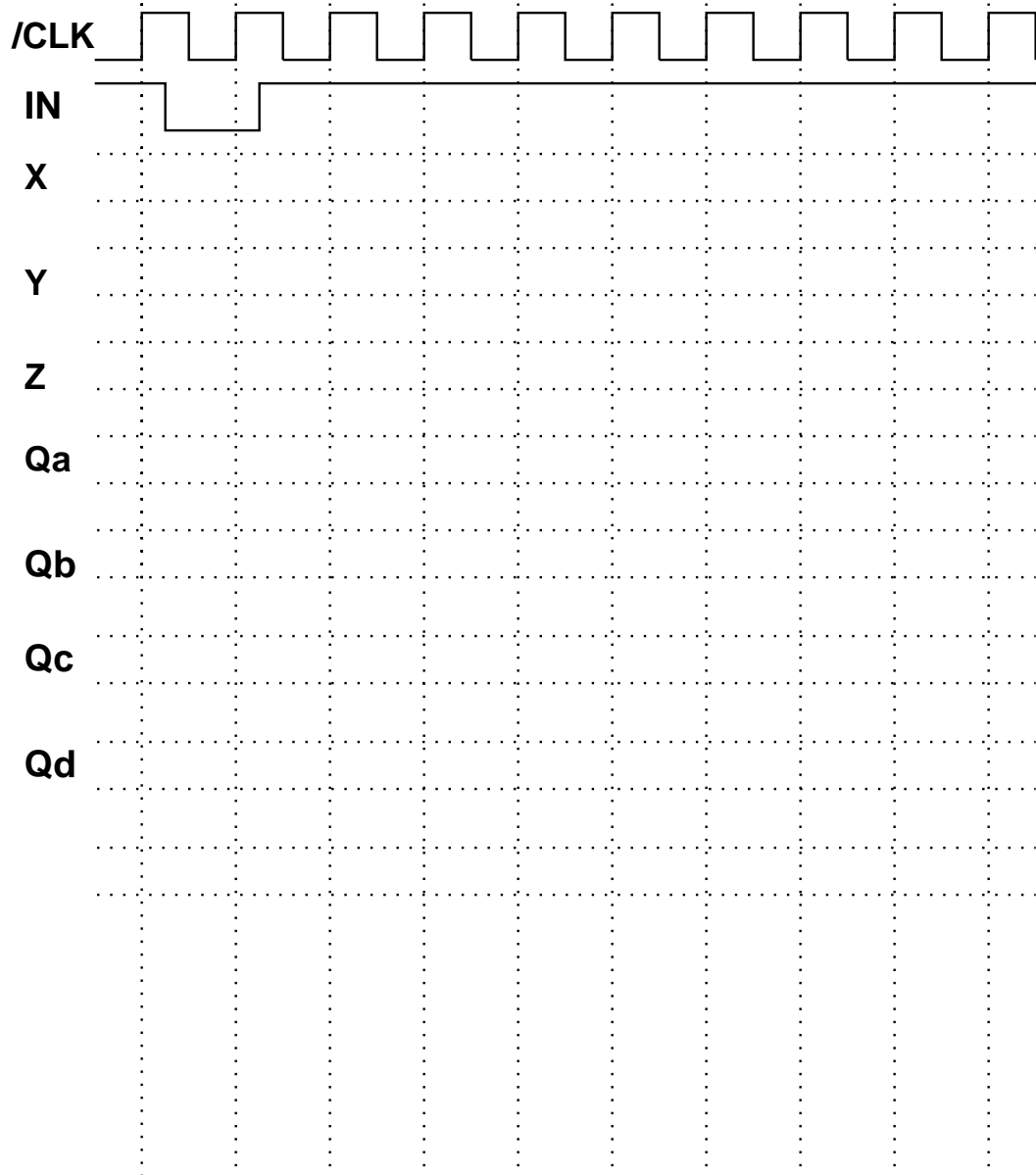


Figure 3b

**Problem 4** (30 points)

a) Implement a JK flip-flop with a D flip-flop and any number of any type of gates on Figure 4a. Maximum credit is reserved for implementations that use the minimum number gates. Of course, correctness of the implementation is paramount.

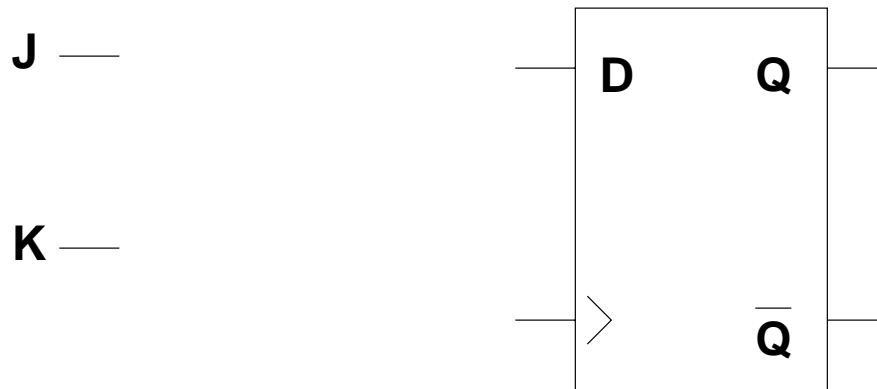


Figure 4a

b) Sometimes it is desirable to count in a Gray code sequence such as that used to label the rows or columns of a Kmap. You are to implement a two-bit gray code counter using the flip-flops shown below. You should assume the counter “wraps around”, i.e., the state after  $Q_1 = 1$  and  $Q_0 = 0$  is  $Q_1 = 0$  and  $Q_0 = 0$ .

First give the truth table for the flip-flop inputs,  $D_0$ ,  $J_1$ , and  $K_1$ .

$Q_1$	$Q_0$	$J_1$	$K_1$	$D_0$
0	0			
0	1			
1	1			
1	0			

Second complete the logic diagram in Figure 4b using any number of any type of gates. As above, maximum credit is reserved for implementations that use the minimum number gates. Of course, correctness of the implementation is paramount.

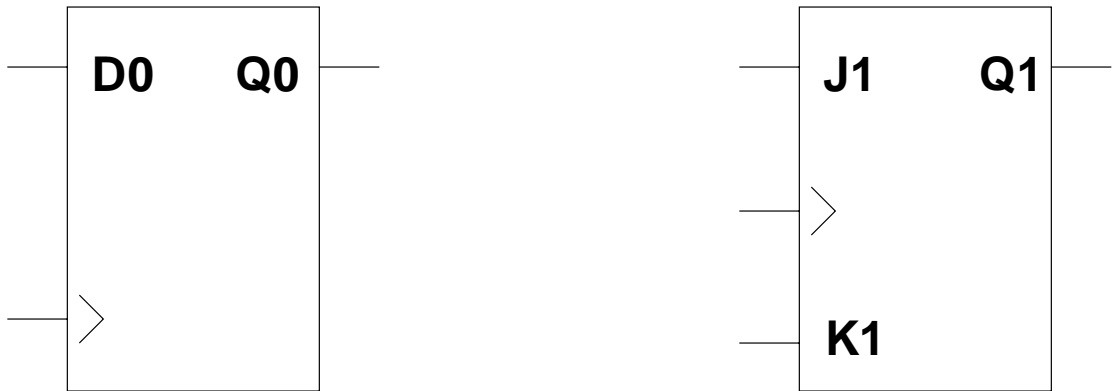


Figure 4b