



## Quiz Review Video



## Quiz 2 Review



### ■ Wednesday, April 9, 2003

- 1:00 to 2:00 (class time)
- Room 50-340 (Walker)
- Closed Book

### ■ Coverage is to Lecture 17

- Emphasis on Lecture 8 – 17

### ■ Topics are:

- FSMs
  - state registers
  - combinational logic
  - VHDL implementation
- Synchronization
  - Short pulse catcher
  - Level to a pulse
- Tristate
- What it is
- VHDL implementation



## Quiz 2 Review - 2



- **More topics**
  - **Avoiding glitches**
    - Gating the clock
    - Registering the output
  - **Miscellaneous VHDL**
    - Don't cares
    - Concatenation - &
    - Operands and result are of the same length.
  - **Hierarchical design**
  - **Start with one block.**
    - Subdivide until blocks are simple.
    - Implement blocks in VHDL.
    - Test the blocks.
    - Wire the blocks together by instantiation.
    - Test the complete design.
  - **Arithmetic**
    - Representation of negative numbers
      - sign – magnitude
      - Ones complement
      - Twos complement



## Quiz 2 Review - 3



- **More arithmetic**
  - Adders
    - Ripple carry
    - Carry look ahead (idea – not details)
  - Shift and add multiplier
- **Reconfigurable logic architectures**
  - Anti-fuse versus RAM-based FPGAs
  - Combinational logic implementation
  - Carry chain
- **Major – minor FSMs**
  - Simultaneous operation
  - Can different clocks be used?
- **Analog building blocks**
  - Op Amps
  - D to A
    - Glitching
    - R -2R ladder
  - A to D
    - Successive Approximation
    - Flash



## Quiz 2 Review - 4



- Data Transmission
  - Serial protocol
  - Parallel protocol
  - Transmission line
    - Termination – characteristic impedance
    - Crosstalk – ground alternate wires
- Custom VLSI Integration
  - Fixed coefficient multiplication
  - Transforms
    - Canonical signed digits
    - Algebraic
      - ❖ Commutative
      - ❖ Distributive
      - ❖ Associative
      - ❖ Common sub-expressions
    - Retiming
      - ❖ Moving delays
      - ❖ Pipelining



## Design Rules



- Use hierarchical design.
  - Small subsystems are easier to design.
- Design for testability.
  - Design subsystems so they will run alone.
  - Design in break points.
  - Design test FSMs as enabled by switches.
- Do your logic design carefully, and first.
  - Make up block and circuit diagrams with pin numbers.
  - Use names appropriate to the assertion levels.
- Avoid problems from 'glitches'.
  - Gate delays can (and do) cause glitches.
    - Ensure a stable combinational output before it is sampled by CLK.
  - CLK, G, /PR, /CL inputs must NOT have glitches.
  - Create glitch-free signals by
    - Registering outputs.
    - Gating the clock.



## Design Rules - 2



- **Use the same clock edge for all edge-triggered flip-flops.**
  - Beware of clock skew.
  - Use a tree structure to expand the clock.
  - Change inputs only (just) after the clock edge.
- **Avoid tristate bus contention.**
- **Be careful about Asynchronous events.**
  - Synchronize all external signals.
  - Consider pulse width carefully.
    - Should you have a short pulse or a sustained level?
- **Use memory properly**
  - Avoid high Z address to SRAM when CE is asserted.
  - Avoid address changes when WE is true.
  - Make sure your write pulse is glitch free.
  - Use a logic analyzer or a scope.
    - Don't use the logic probe in the lab.



## How to Make Your Project Work



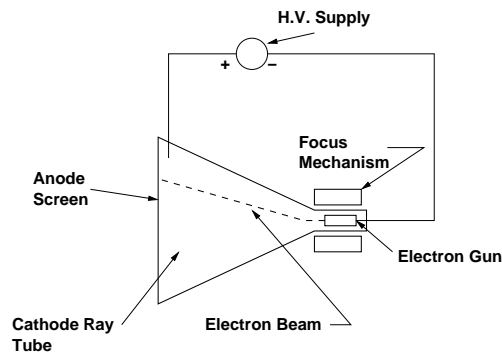
- **Read (and heed) all of the handout.**
  - It is 'old' but all of it is good advice.
- **Sections that are particularly relevant are:**
  - Wiring Errors
  - Care and Feeding of the Power Supply
  - Unused Inputs
  - Behavior of Ungrounded Parts
  - Tri-State Logic Signals
  - Handling CMOS Parts
  - Wire Routing
  - Clock Distribution
  - Gating the Clock
  - RAM Write Pulses
  - Synchronizer Errors
  - Testing Strategies
  - Driving High Current Devices



## Video Displays



- Video displays are implemented by mirrors, LCDs, and CRTs.
- In a CRT (the displays in our laboratory)
  - electron beams are focused on a small spot on the screen.
  - The energy delivered to a phosphor causes a dot (pixel) to glow.
    - The beam can be moved rapidly in two dimensions.
    - The beam current determines the brightness of the spot.



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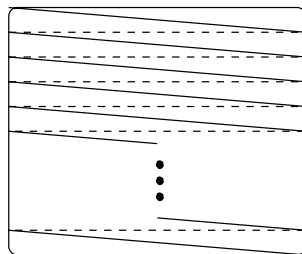
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## Raster Scan



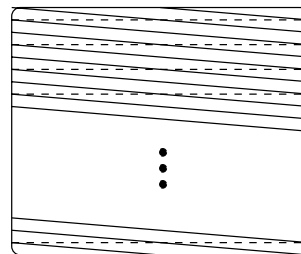
- Television and most computer displays use raster scan.



Non-Interlaced: Frame rate may be 60, 72, etc. frames/sec.

———— Scan line  
 - - - - - Retrace line

Electron beam "scans" tube. Beam location is shown here. Beam current determines brightness of display.



Interlaced: Frames alternate. This is like television: 60 half frames/sec.

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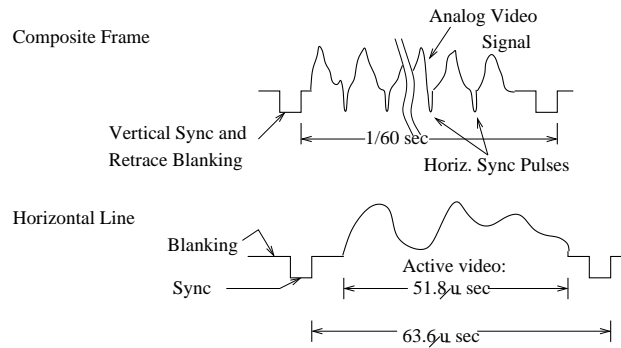
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## Composite Frames



- The 'frame' is a single picture (snapshot).
  - It is made up of many lines.
  - Each frame has a synchronizing pulse (vertical sync).
  - Each line has a synchronizing pulse (horizontal sync).
  - Brightness is represented by a positive voltage.
  - Horizontal and Vertical intervals both have blanking so that retraces are not seen (invisible).



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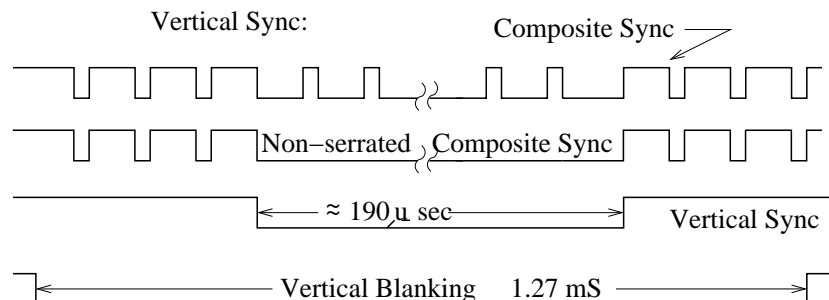
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## Composite Synchronization



- Horizontal sync coordinates lines.
- Vertical sync coordinates frames.
- They are similar except for the time scales and they are superimposed on each other. The numbers are for TV-like displays.
  - What purpose is there for serrated sync?



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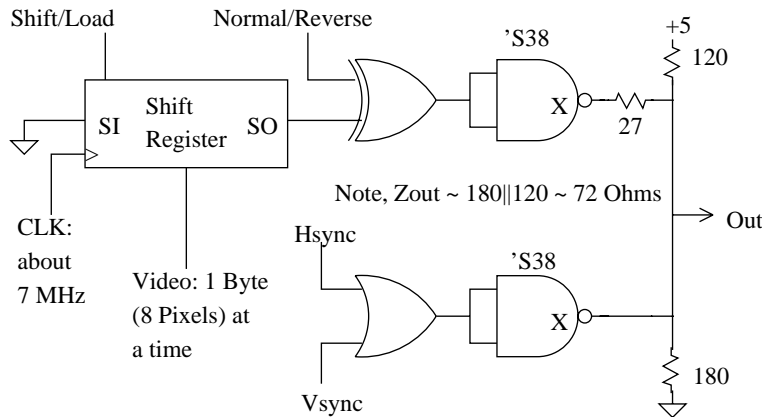
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## Generation of Signals



- Assume one bit per pixel and provide for reverse video.
- This is a simple 'D/A' to generate monochrome signals.
  - The 'S38 is an open collector part so the voltages are determined by the resistor network. The output resistance is ~ 75 ohms.



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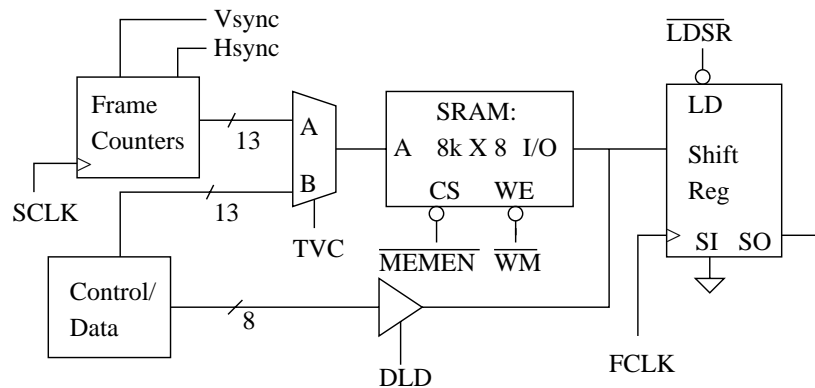
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## Control



- Here is one possible display format.
  - 256 pixels X 192 rows
  - 7.16 MHz clock => 140 nanoseconds per pixel
  - Display time for the active line is 35.8 microseconds.
  - $256 \times 192 = 49,152 = 48K$  pixels = 6 K bytes



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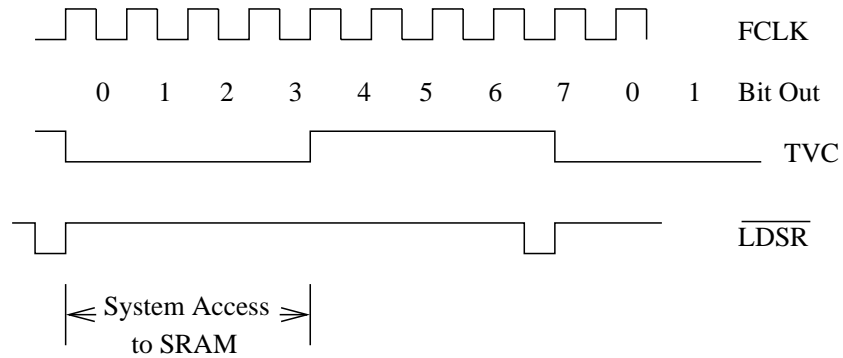
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## Timing of Control Signals



- Data is loaded into a shift register and shifted out to generate the video signal.
  - FCLK is at the pixel rate.
  - TVC divides access to the SRAM giving half the time to get data to load into the shift register .



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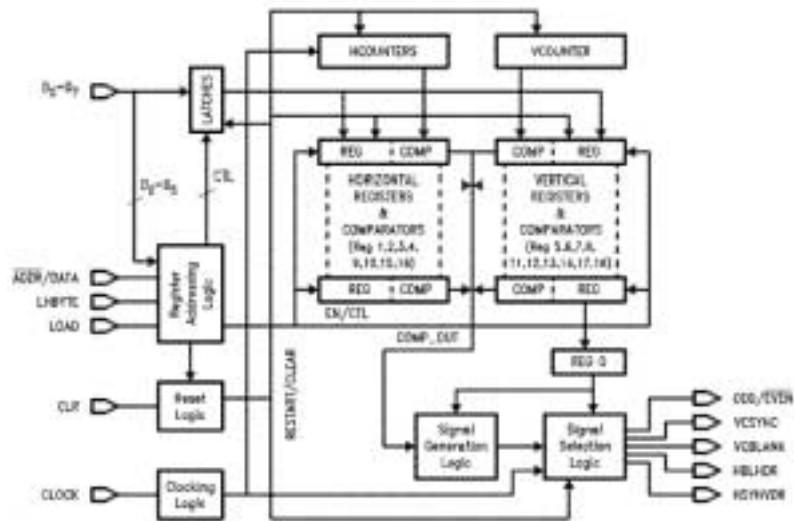
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## LM 1882 Sync Generator



See web page. – Look under Resources.– Click on Video sync.



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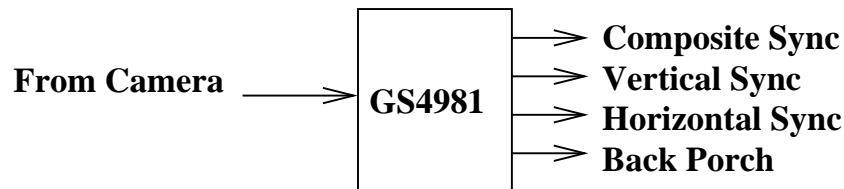
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## Sync Separator



- A sync separator operates in the reverse direction.
  - GS4981 generates composite sync from video.
    - It also generates separated sync signals.
- However, your pixel clock must be synchronized with the recovered horizontal sync.
  - If you do this synchronization with the pixel clock signal directly, then the pixel clock used will “crawl” a whole pixel time.
  - It is better to use a faster clock, say 4 times, to do the synchronization and then the “crawl” will only be  $\frac{1}{4}$  of a pixel time (distance).



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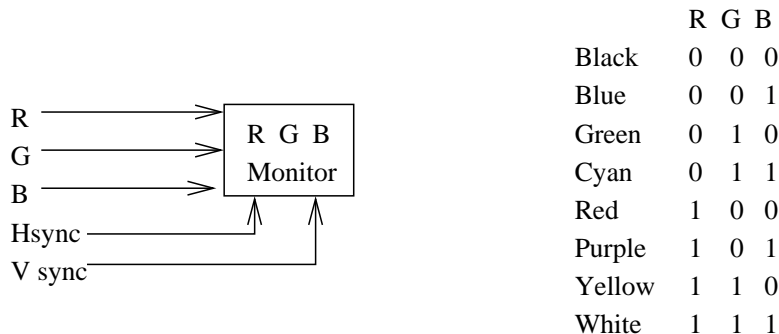
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## Color Displays



- Color displays are similar to three monochrome displays operated together, i.e., the colors add.
- Three binary signals yield an eight-color display.
  - Some monitors have an analog video input for each color.
- Sync is sometimes on a separate wire.
  - Sometimes it is superimposed on the green signal.



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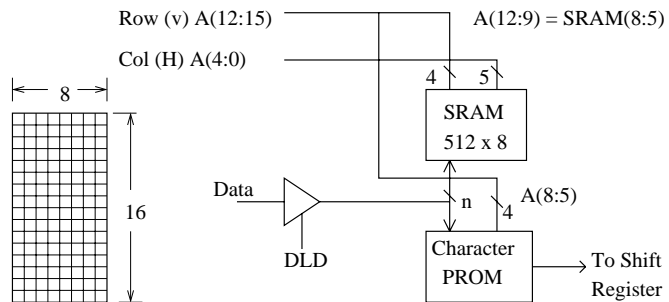


## Character Display (8 x 16 pixels)



- Characters are fixed bit patterns.
  - They always have the same shape but can appear at different places on the screen.
  - Use of characters can save video memory and make the manipulation of video memory contents simpler.

For a screen  
256 x 192 one  
gets 384  
characters.  
The screen  
address is used  
to specify the  
position and  
part of the  
address of the  
character ROM



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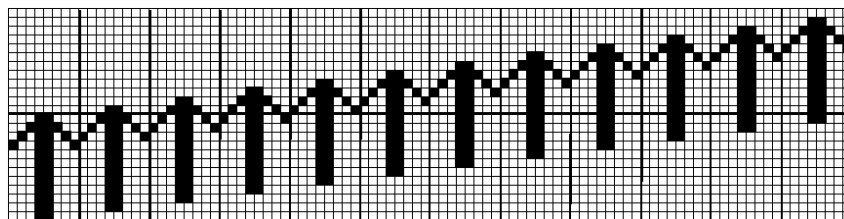
19



## Pairs of Characters



- Sometimes, pairs of characters can create the same motion effect as bit-mapped graphics.
  - The speed of the motion depends on the update rate.
- These 24 characters (12 x 2) can display an arrow at any vertical position.



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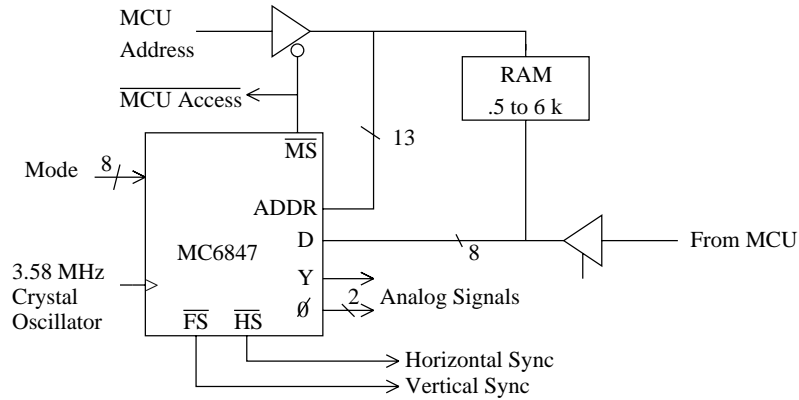
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## Video Controllers



- **MC6847 is obsolete but easy to use.**
  - It provides a 13-bit address and an analog video signal.
  - It reads 8-bit data which can be either a character code or video data.
  - Several display modes include 256 x 192 two-color and several other color graphics modes with lower resolution.



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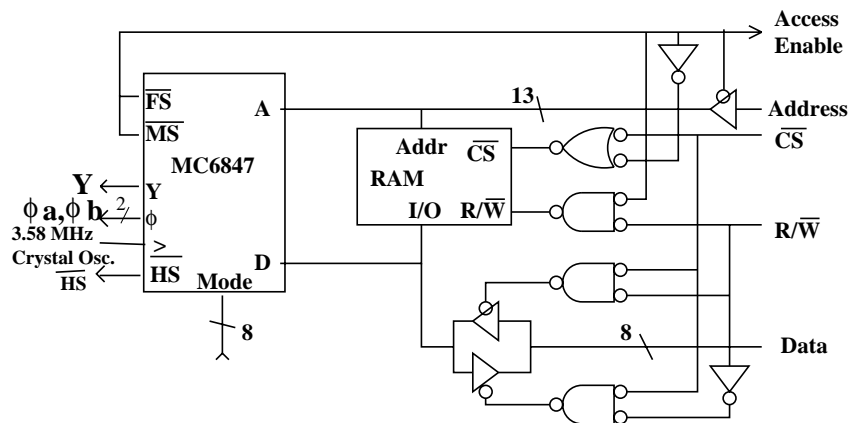
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## Bit-Mapped Video



- **MC6847 can be used with bit-mapped video.**
  - More about Y, phi A, and phi B later.



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## MC6947 With a Character ROM



- You can call it a bug or a feature!
  - To get around the fact that /RP begins and ends between /HS pulses, one must use a counter that has an asynchronous clear, similar to the '161. Of course, one can implement this counter with VHDL but one has to remember to implement an asynchronous clear.

