

Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science

6.111 – Introductory Digital Systems Laboratory  
Problem Set 3

**Issued: February 19, 2003**

**Due: February 26, 2003**

### **Problem 1: Counters**

Design a the following 4-bit counters with logic and LS163s

- (a) Counting up even numbers: 0,2,3, etc
- (b) Counting down odd numbers: 15,13, etc.
- (c) Increasing even numbers and Decreasing odd numbers: 0,15,2,13,4,12, etc.

### **Problem 2: FSM**

Design a finite state machine with an asynchronous reset that outputs a '1' after receiving the string, '011', and outputs '11' after receiving the string, '100.

- (a) Draw and label the state diagram. Use the minimum number of states.
- (b) Implement your FSM in VHDL and simulate using Max+plus II.

### Problem 3: T Tokens

Here you will design a machine that will dispense T tokens. Your inputs will be the money -  $X=0$  for quarters, and  $X=1$  for one dollar bills. Another input will be the number of tokens needs, N, which is a 2-bit number with the values - 00(for one token), 01(for 2 tokens), 10(for 3 tokens), and 11 (for 4 tokens). Your output will be the number of tokens dispensed. No change will be given, and T tokens are 1 dollar. Don't forget to include a reset.

- (a) Give the state transition table.
- (b) Draw and carefully label the state diagram.
- (c) Implement in VHDL and print out your simulation.
- (d) Implement using logic and D flip flops.