

Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science

6.111 - Introductory Digital Systems Laboratory, Spring 2003  
Problem Set 5

Issued: March 12, 2003

**Due: March 21, 2003**

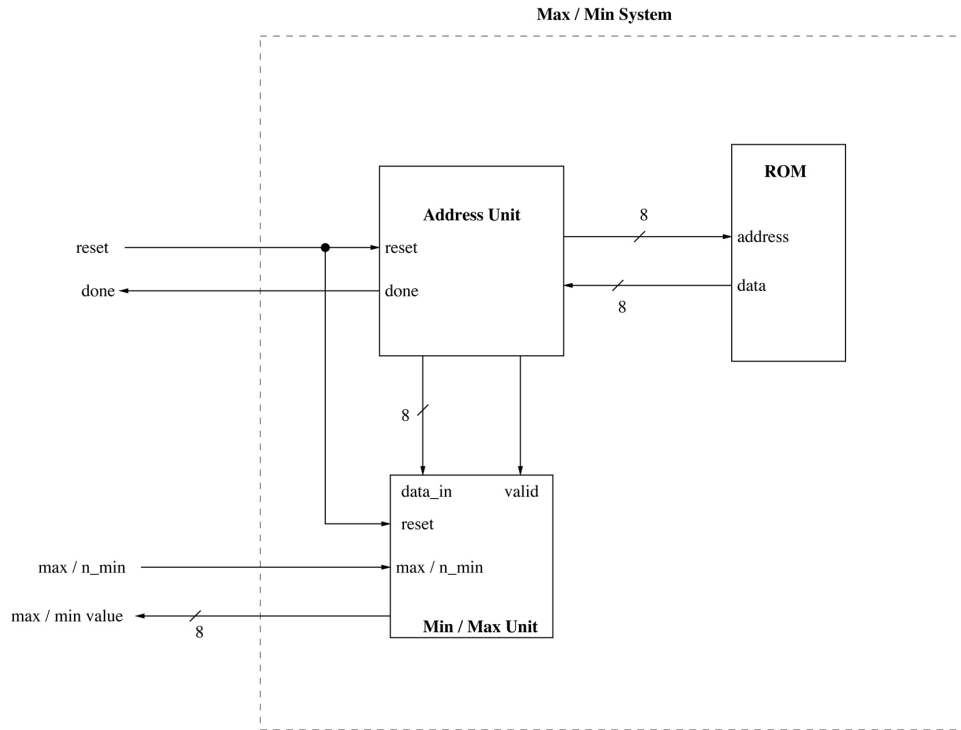
In this problem set you will design a system that takes a sequence of unsigned integers and determines the maximum and minimum integer in the sequence.

Each integer is an 8-bit unsigned number; The sequence of integers is stored in an 8x256 ROM in the following linked-list type format:

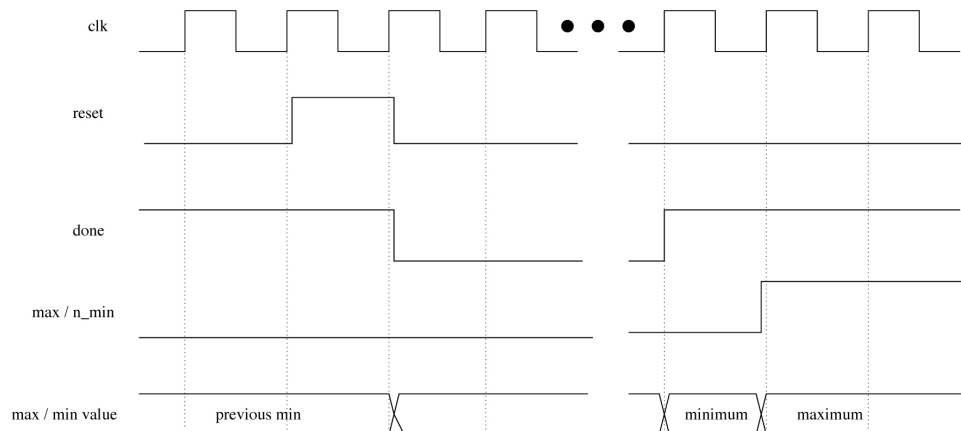
The ROM contains a number of entries. Each entry consists of two 8-bit numbers stored in consecutive addresses. The number in the first address is part of the list of integers over which we are seeking the max and min number. The number in the second address is a pointer to the next entry in the ROM. The first entry in the ROM is assumed to be at address 0x00. A pointer value of 0x00 indicates that that entry is the last one in the sequence. A sample ROM contents is shown below.

ROM address	Address contents
0x00	0x03
0x01	0x05
0x02	???
0x03	???
0x04	???
0x05	0x13
0x06	0x0A
•	•
•	•
•	•
0x0A	0x10
0x0B	0x20
•	•
•	•
•	•
0x20	0x56
0x21	0x00

In the above sample ROM, the numbers in the sequence over which we want to determine the max and min are 0x03, 0x13, 0x10, and 0x56.



The above figure shows a block diagram of the system. After the reset signal has been asserted, the system should begin its computation. Some number of clock cycles later, the done signal will be asserted and will stay asserted until reset is again asserted. Once done is asserted, if max / n-min is 1 then the maximum integer appears on the max / min value bus; if max / n-min is 0 then the minimum integer appears on the max / min value bus. A timing diagram is shown below.



Design the Addressing and Min / Max Units. Include block diagrams of the internal components of the units. Design at the block diagram level—do not design at the gate level (though you may have to include a few gates in your block diagram). If you use an FSM for the control in a unit (you may not have to for both) then include a state transition diagram. Implement the two units in vhdl, and simulate the Max / Min unit. Be sure to include a printout of your simulation. You do not have to turn in simulation waveforms for the addressing unit.